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Issue 2/2008

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A TOUGH DECISION

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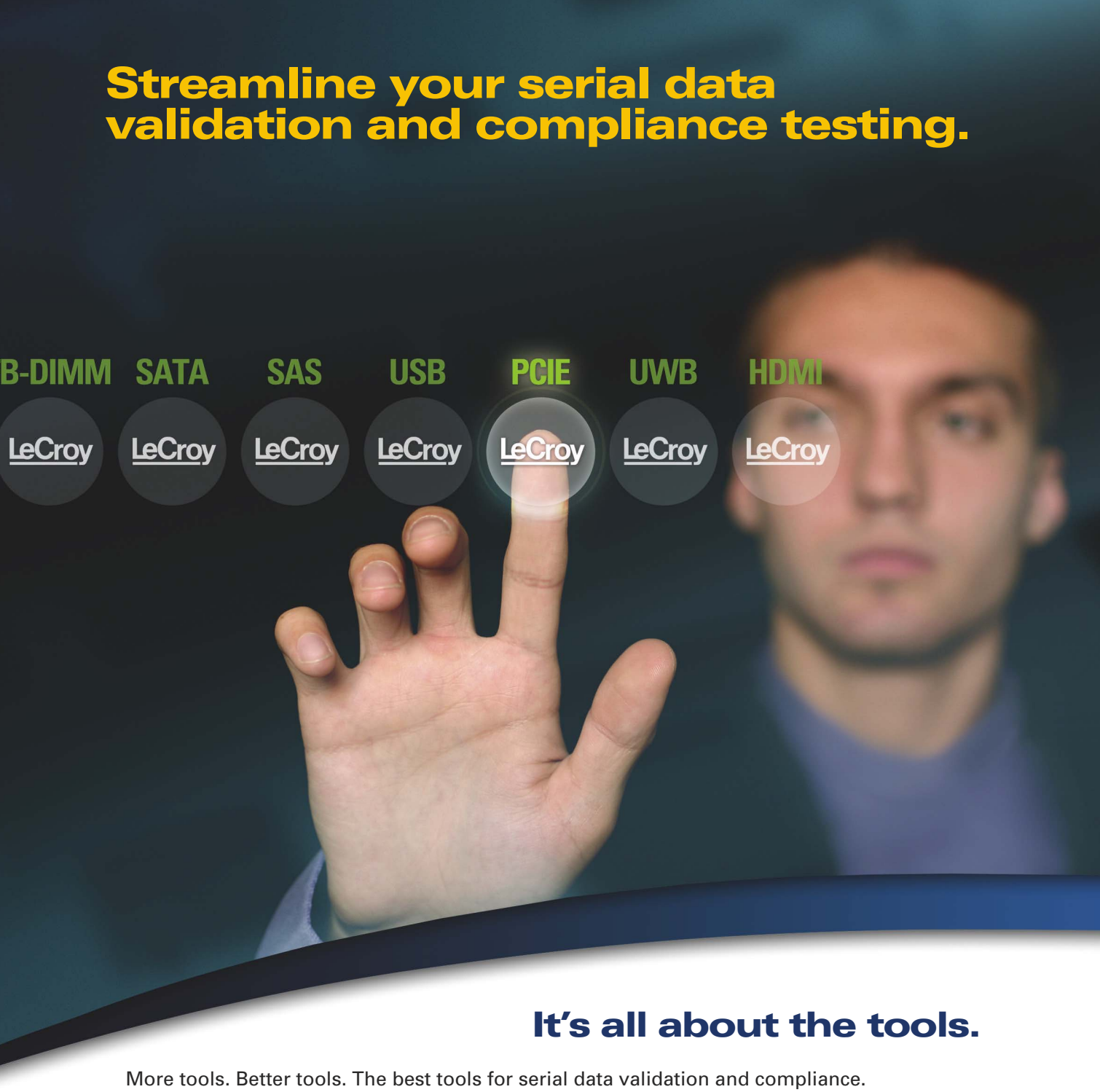
Streamline your serial data validation and compliance testing.



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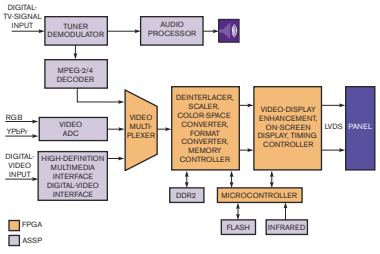
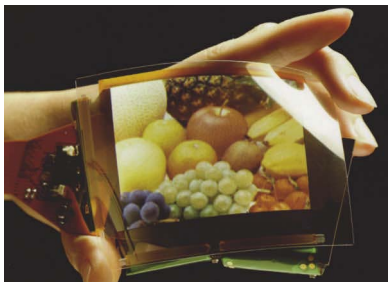


Using FPGAs for HDTV design

Choosing system-on-chip processes: a tough decision



Digital video pushes the embedded-technology envelope

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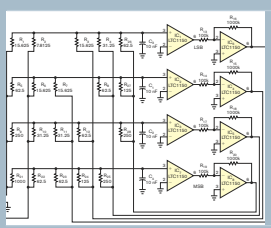

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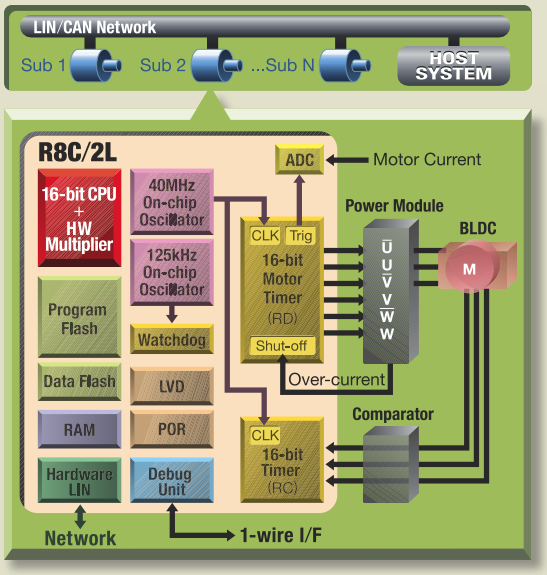

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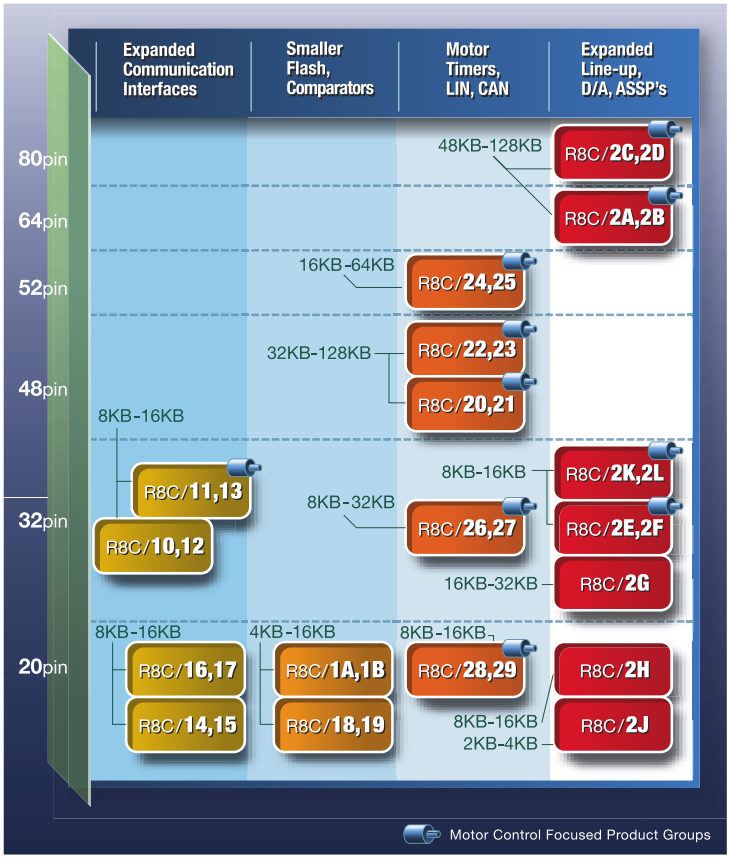

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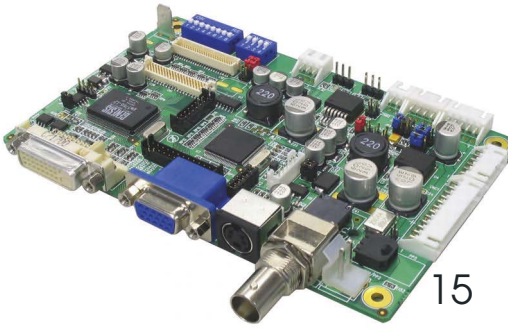

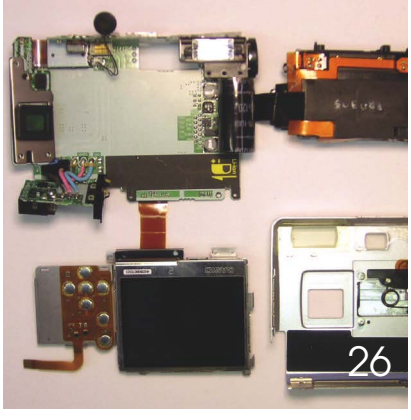

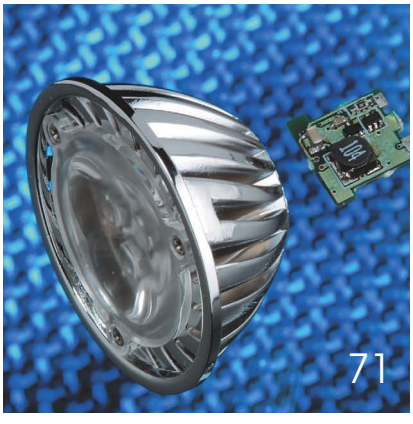

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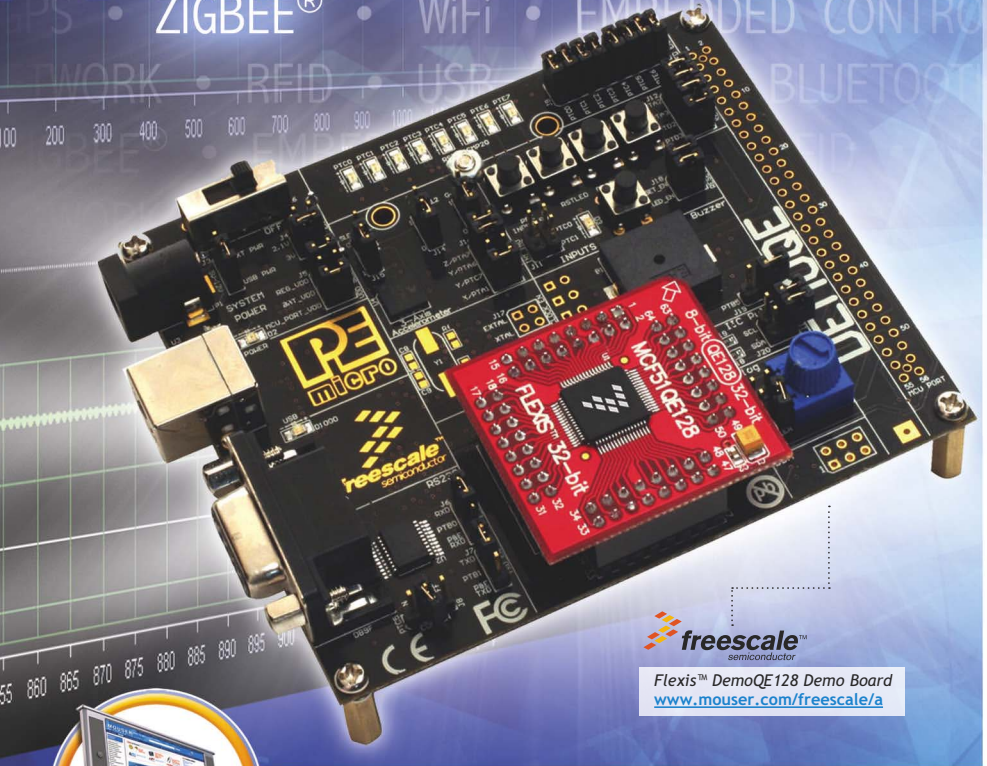

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BY PAUL RAKO, TECHNICAL EDITOR

Overengineering: How much is too much?

Veterans Day 2007 brought to mind a story my father once told me. He was in the US Army's 8th Engineering Corps Division. His unit saw fierce fighting in Hürtgen Forest during World War II. He told me that Germany's battlefield telephone lines used sheathed-wire pairs in clamshell enclosures. A small lever energized a machined, cam-operated mechanism that smoothly slid the connector halves into engagement. Allied soldiers had standing orders to shoot through the engineered connectors and to cut the cable with their bayonets.

In contrast, the engineers who had strung the wire for the US field telephones left a few feet of loop every hundred yards, so that slack would be available to fix even large breaks. The current loop closed through the earth; only one olive-drab, insulated-iron wire connected to the phones. The Army used iron because it was more resistive and stronger than copper; that strength was necessary to withstand the hardship of soldiers' pulling it off the spools to the front lines of battle. Allied soldiers who encountered cut US-telephone wires had orders to use their bayonets to remove the insulation and tie the broken wires into knots, tugging hard to make good connections. They then threw the wire back into the ditch or bomb crater.

As soon as the Germans had to retreat or give up ground, the US soldiers made sure that the German phones would not work for weeks or months.

The results of these two engineering approaches became evident in the toughest fighting in Europe. If everything went according to the Germans' plan, their telephones worked far better than US phones. As soon as the Germans had to retreat or give up ground, however, the US soldiers made sure that the German phones would not work for weeks or months. The Germans didn't have enough clamshell connectors in warehouses to replace all those that US soldiers had destroyed with their weapons. The exact opposite scenario happened with US field telephones. When the US military gave up ground, the Germans cut the wires, but, as soon as any Allied troops retook the ground, they tied those knots and once again had working phones.

Certainly, the specs for the German phones were far superior. The signal-to-noise ratio and fidelity were fabulous. But those great specs were of little use when the phones didn't work. The US phones worked well enough in real-world battlefield conditions. The German phones were overengineered, which brings me to my point on overengineering: Good design is about making compromises on a continuum of choices. That fact describes analog design, and analog design is what life is all about. I don't really need 700 menu selections on a BMW iDrive joystick. EDN

Contact me at paul.rako@reedbusiness.com.

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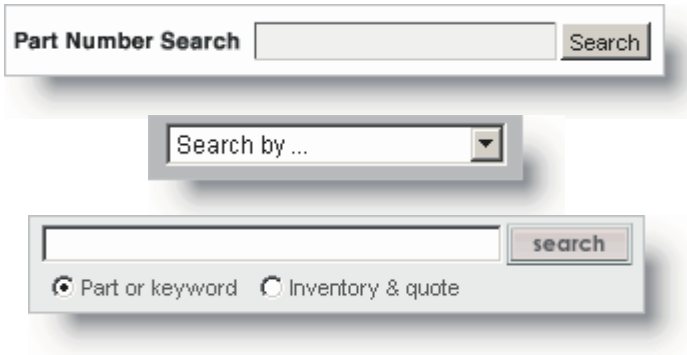

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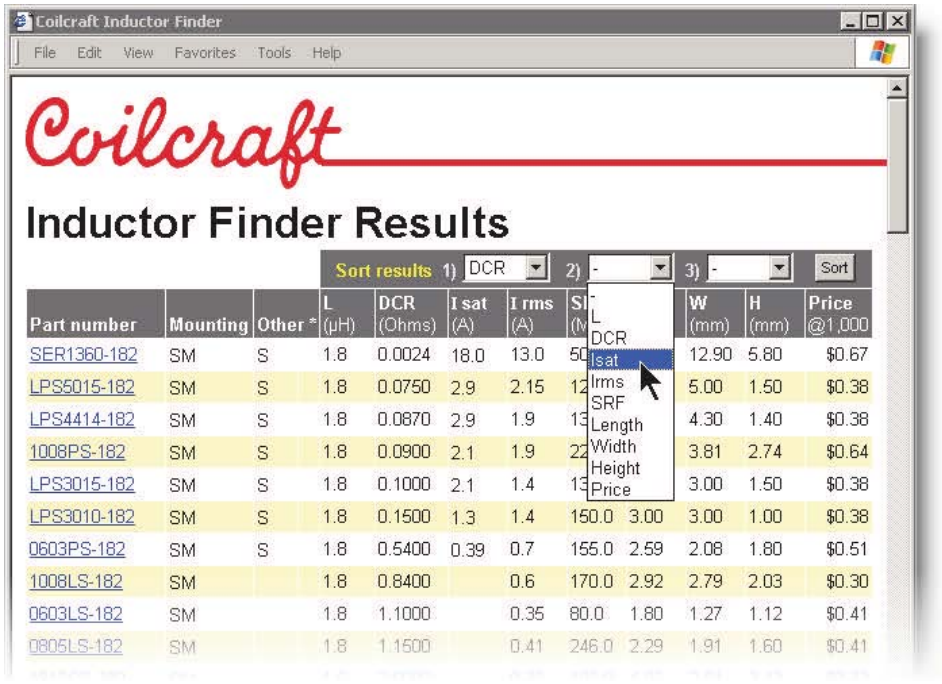

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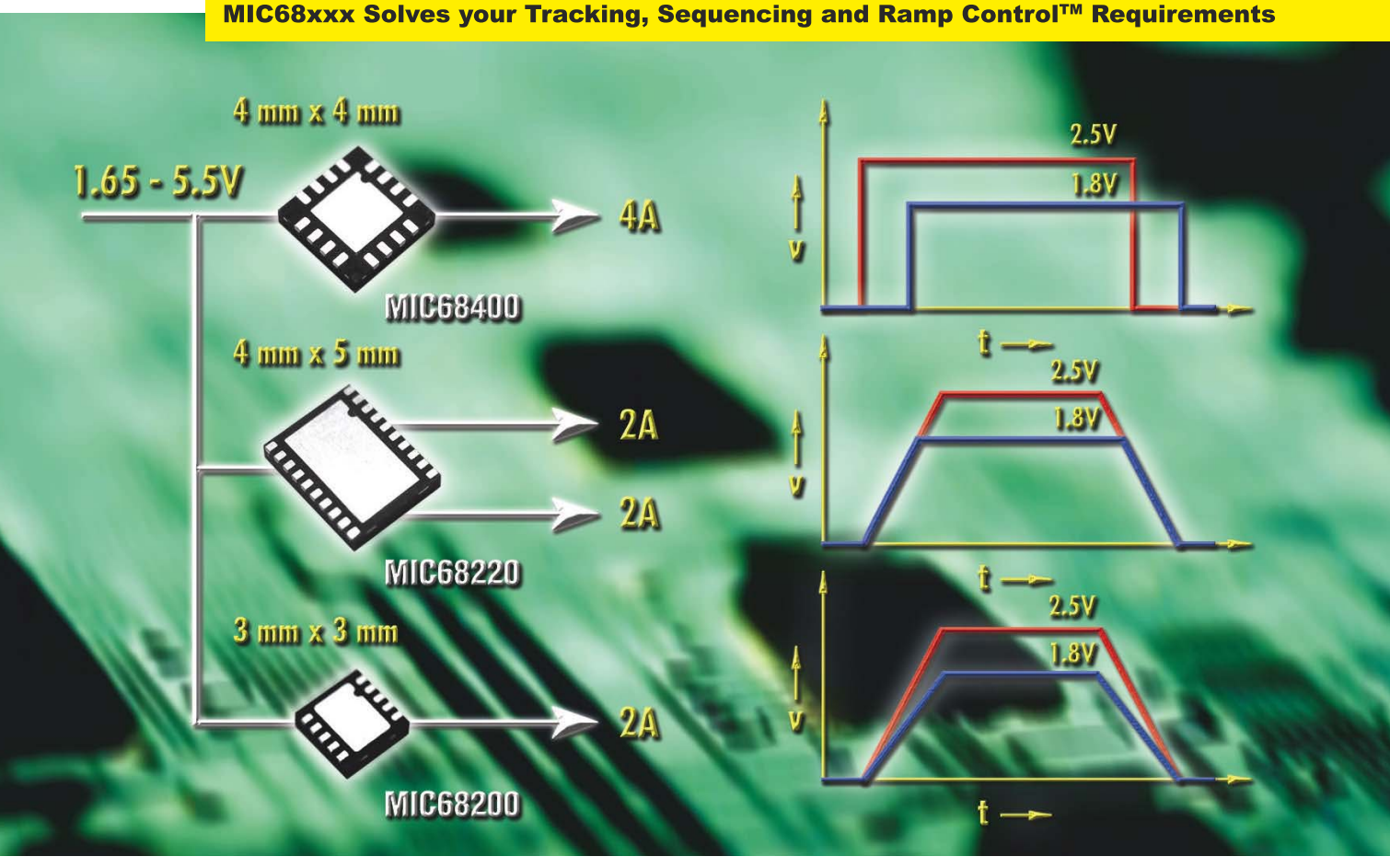

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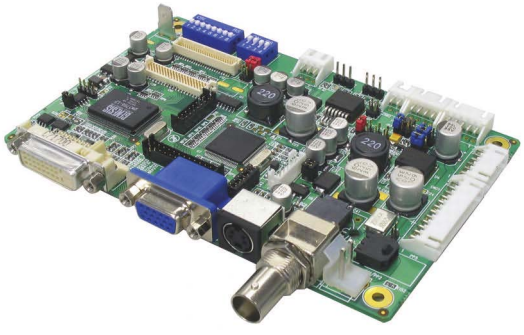
INNOVATIONS & INNOVATORS

LCD controller serves multiple monitors

The new DVS-1600 interface controller from Digital View addresses a variety of TFT (thin-film-transistor)-LCD-monitor applications with support for multiple input connectors, video protocols, and LCD panels. The board's port architecture provides physical inputs for DVI (Digital Video Interface), VGA, S-Video, and composite video, along with corresponding signal-processing modes. The DVS-1600 comes preprogrammed to drive several panel models and resolutions that are selectable via onboard DIP switches. The controller supports panel resolutions from VGA (640×480 pixels) to UXGA (1600×1200 pixels), as well as panel formats of 4:3, 5:4, 16:9, and 16:10.

You can update timing and video-processing features as necessary through the controller's serial port. Other features of the DVS-1600 include built-in support for multiple VESA (Video Electronics Standards Association) timing modes, plus legacy-video modes, such as synchronization-on-green and composite synchronization. The DVS-1600 is available now for $110 (1000).**—by Warren Webb**

▷**Digital View**, www.digitalview.com.



The DVS-1600 interface controller supports multiple input connectors, video protocols, and LCD panels to simplify the development of LCD applications.

FEEDBACK LOOP

"As for the mention in the article about trying to impress one's cute cousin, I'm not so sure about that. I'd rather impress someone else's cute cousin!"

—Reader Scott B discusses family matters in *EDN*'s Feedback Loop, at www.edn.com/article/CA6495303. Read the column and add your comments.

ARM targets NFC smart cards with Cortex variant

With its SC100 SecurCore processor IP (intellectual property), ARM believes that it has the largest share of the approximately 50 million-unit-per-year market for secure smart-card processors. ARM licenses the IP to 12 silicon vendors, and SIM (subscriber-identity-module) cards represent the biggest application category for it. ARM is now updating that offering with the Cortex M3-based SC300, which it designed for incorporation into USB and contactless smart cards. It employs the Thumb 2 instruction set and, the company says, provides twice the performance/energy factor of its predecessor. ARM also provided it with real-time handling of multiple interfaces for high-speed and contactless applications, including smart-card Web servers and NFC (near-field communication).

The company expects the use of multiple-application cards, such as large memory cards with secure interfaces, to proliferate in the growing base of NFC applications, according to Richard York, product manager. Designers use these cards to host, for example, media and music storage, and the processor must be able to support media streaming while conducting secure transactions. The SC300 provides the resources to perform these tasks. By limiting the gate count and providing the ability for licensees to tune the processor's configuration, ARM created a silicon-and-code footprint that is no bigger than an 8-bit chip. "The energy efficiency of the SC300 is the real justification of the product," says York. The development-tool chain is "standard ARM," he notes, and a DLL (dynamic-link library) models the processor in a smart-card simulation. You can then simulate a smart card on a PC in real time at 10 to 20 MHz and physically connect the simulation to a card reader. The smart-card world is still largely based on proprietary architectures. With the SC300, ARM hopes to convert silicon vendors to ARM's approach.

—by Graham Prophet

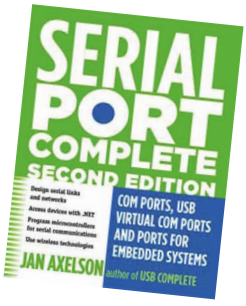
▷**ARM**, www.arm.com.

Book delves into serial ports; they never were "obsolete"

A recently published book addresses the need for and popularity of serial ports. *Serial Port Complete Second Edition* (Lakeview Research, December 2007, ISBN 978-1931448-06-2) by Jan Axelson explores hardware and software; ports in PCs and embedded systems; and RS-232, RS-485, and wireless interfaces. Axelson banishes the myth that serial ports are obsolete. She describes how, when the USB interface took hold in the late 1990s, many in the industry made this prediction. Although plenty of peripherals that formerly used the serial port have switched to USB, some devices can't use USB or have requirements that USB alone can't provide. As a result, many embedded systems use serial ports because they're inexpensive and less complex to program than USB ports and can use longer cables than USB allows. Also, the RS-485 serial interface supports networks for many monitoring-and-control applications. Although most PCs no longer have built-in serial ports, you can easily add them with USB converters, meaning that the number of expansion slots no longer limits the number of serial ports a system can have. Microsoft's (www.microsoft.com) .NET Framework SerialPort class lists a large number of ports, indicating that PC applications continue to find communication ports useful.

The first chapters focus on hardware and interfacing and introduce asynchronous-serial communications. Chapter 3 discusses serial ports in PCs, and chapters 4 through 8 provide a guide to interfacing using RS-232, RS-485, and wireless technologies. The following chapters provide a guide to programming. Axelson also describes how to program serial ports on PCs using Visual Basic .NET and Visual C# .NET. Later, she shows how to program serial ports for embedded systems with examples for MicroEngineering Labs' (www.microengineeringlabs.com) PICBasic Pro compiler and Microchip Technology's (www.microchip.com) MPLab C18 C compiler. The $39.95, 380-pg book also covers hardware and programming for RS-485 serial networks and how to implement USB virtual-communication ports using special-purpose and generic USB controllers.

For the second edition, the author has revised and updated the contents. For example, she adds code in C/C# as well as in Basic and includes code examples for PCs and embedded systems. The book also covers designing and programming USB virtual-communication ports, using wireless technologies to transmit serial data, accessing serial ports over Ethernet or Wi-Fi networks, and transferring text data using Unicode encoding. Whether your interest is hardware or software and whether you work with PCs, embedded systems, or both, you'll find useful guidance in this book. Programmers will learn how to communicate using serial ports, including USB virtual-communication ports, in PCs and embedded systems. The sample code for PCs and microcontrollers in Basic and C/C# provides a quick start for a variety of applications. Circuit designers will find designs for a variety of applications, including converters that translate between RS-232, RS-485, and 3 and 5V logic. The book also includes designs with fail-safe features, high noise immunity, and low power consumption.



The book provides hobbyists and experimenters with inspiration for projects and enables teachers and students to learn about serial ports and use the examples in this book to demonstrate concepts. This book assumes a basic knowledge of electronics and either Basic/Visual Basic or C/C# programming. It assumes no previous knowledge or experience with serial-port hardware or programming.

—by Dan Strassberg

▷**Lakeview Research**, www.lvr.com.

FEEDBACK LOOP

"The professor started off as follows: 'You are now starting your career in electronics. At Sunday lunch, Aunt Judy will ask you to fix her radio. Take the radio, and ... apply full ac across the battery terminals and destroy it completely. Within hours, your entire extended family will know how useless you are, and you can complete your college education without having to do annoying favors for friends and family.'"

—Reader Paul Michelow, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6495303. Add your comments.

DILBERT By Scott Adams

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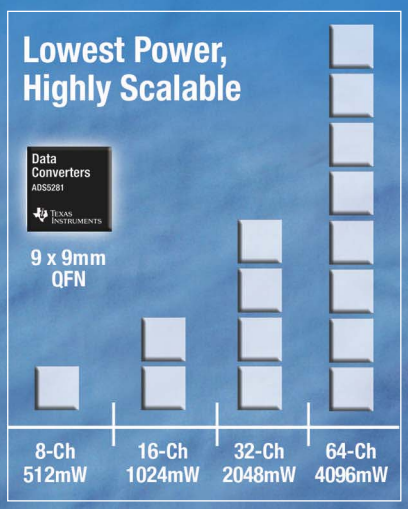

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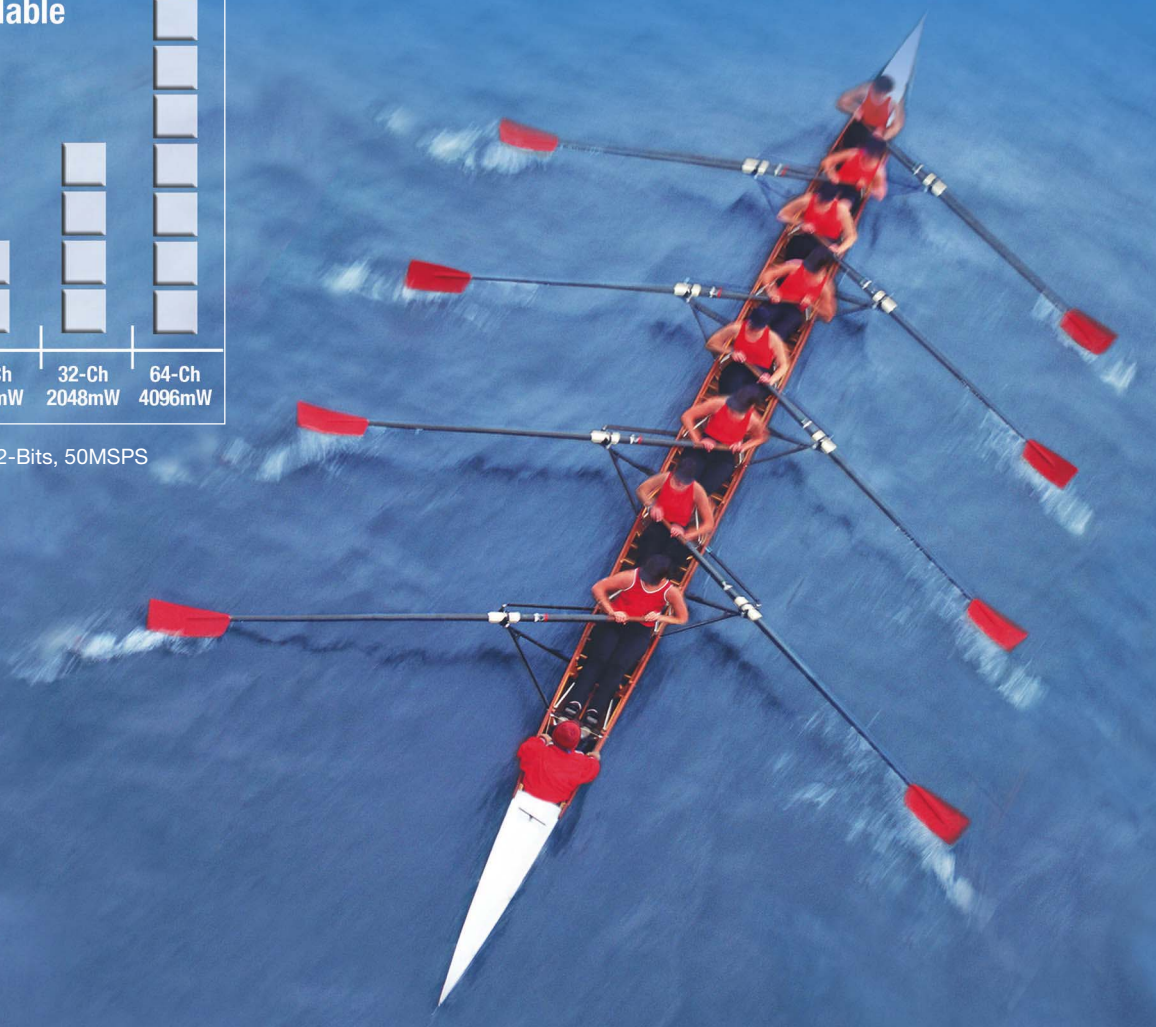

Texas Instruments

Processor and tool enhancements include real-time trace

All Tensilica configurable processor cores now support an optional nonintrusive real-time-trace block that includes the hardware and software necessary for tracing software-program execution. The Nexus 5001-compatible Trax-PC trace macrocell supports real-time implementation in silicon and in FPGAs. Software-debugging support includes visualization tools through Tensilica's Xplorer. The trace block compresses the data from the trace port and buffers the compressed data in a user-supplied trace buffer, which users can access from outside the system through the JTAG TAP (test-access port). The Trax-PC can trace all changes in program flow, including exceptions and interrupts, and it can accept PC-based external-trigger inputs. The host software decompresses the trace data, reconstructs the program execution, and provides annotated program-disassembly and application-source listings through the Xplorer debugger.

Tool-enhancement features include automated generator support for the Xtensa LX2 FLIX (flexible-length-instruction-extension) instructions that manage profiling the application code and suggesting VLIW (very-long-instruction-word) instructions for accelerating the performance of that code. The generator automatically fuses two or three instructions that will execute simultaneously, without requiring the designer to understand how to write TIE (Tensilica-instruction-extension) code. Tool enhancements include a manual fusion editor that graphically assists designers in creating chains or fusions of operations to accelerate code execution. The cycle-accurate ISS (instruction-set simulator) has seen a 15 to 30% speed improvement, depending on whether the designer is using memory modeling. The new dynamic loader allows designers to load binaries in different memory addresses at runtime. The Xenergy energy-estimator tool now includes memory with the core in its energy estimates; it can graphically chart the energy profile for instruction- and data-cache configurations to provide a visual comparison of energy profiles.

> The energy-estimator tool can graphically chart the energy profile for instruction- and data-cache configurations to provide a visual comparison of energy profiles.

The company also recently announced its smallest processor core, the Diamond Standard 106Micro core. The product comes in speed- or area-optimized configurations and can operate as fast as 400 MHz or consume as little as 0.13 mm^2 of silicon in a 90-nm G process. The core uses a 16-entry main-register file instead of a 32- or 64-entry configuration, and it includes support for relocatable exception vectors. The core includes an option for a low-area, multicycle, pipelined, 32×32-multiplication multiplier and software emulation of multiplication instructions as well as an option for a low-area divider. In addition to the AHB (advanced-high-performance-bus)-lite bridge, the core supports an AMBA (advanced-microcontroller-bus-architecture) AXI (advanced-extensible-interface) bridge. These cores are available now for licensing.

—by Robert Cravotta

▷**Tensilica**, www.tensilica.com.

MAXWELL/LISHEN ALLIANCE COULD OFFER IDEAL ENERGY/POWER PROFILE FOR HYBRID VEHICLES

One of the challenges of designing with conventional lithium-ion batteries for HEVs (hybrid-electric vehicles) is that the energy-centric–rather than power-centric–batteries store a lot of energy but are slow to charge and discharge. The relatively new lithium-iron-phosphate batteries are the reverse: They charge and discharge with gusto but can store only a fraction of the energy of conventional lithium-ion batteries.

However, lithium-iron-phosphate batteries are not the only devices with a rapid charge/discharge capability: Ultracapacitors, also called supercapacitors, can charge and discharge large bursts of power over an almost unlimited number of cycles. For this reason, ultracapacitors are popular in hybrid buses and commercial vehicles in which rapid charging and discharging allow the vehicles to use harvested energy from their braking system to charge and then discharge to power or to help provide power during acceleration.

With the goal of producing an efficient energy-storage/power-delivery system for HEVs, Maxwell Technologies, maker of vehicle-sized ultracapacitors, and Tianjin Lishen Battery, maker of lithium-ion cells, have formed an alliance to manufacture and market energy-storage products that combine their technologies. Designers need not know what's inside these products. They could contain batteries, ultracapacitors, a battery/ultracapacitor combination, or hamsters on steroids–as long as the power-system "black box" fits the energy storage/power profile at the required cost and safety performance.

—by Margery Conner

▶Maxwell Technologies, www.maxwell.com.

▶Tianjin Lishen Battery, www.lishen.com.cn.

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TEXAS INSTRUMENTS

8A step-down regulator comes in surface-mount module

Linear Technology has released the latest in its series of dc/dc converters. The company's µModules are complete, packaged power-conversion devices, including inductors, capacitors, and compensation, in a low-profile, molded package with land-grid-array-style contact pads for direct soldering to a PCB (printed-circuit board).

The LTM4608 is part of the µModule family that Linear characterizes as having low input voltage and medium power, according to Afshin Odabaee, product-marketing engineer. With an 8A, 10A-peak current rating, it accepts an input of 2.375 to 5.5V and a maximum of 6V and delivers an output voltage of 0.8 to 5V. The package measures 9×15×2.8 mm; output regulation is ±1%. You can connect multiple modules to supply higher currents. Current sharing is beneficial when you use a simple parallel connection, and all of the chips in such a connection will always start, Odabaee says. You can also chain-clock connections between parallel-connected modules for polyphase operation. The LTM4608 has tracking for controlled ramp-up, ramp-down, and sequencing of the output voltage, as well as output-voltage margining for system-level testing: A power-good output signal tracks the margining to indicate when the output is within limits. You can synchronize the switching to an external clock.

The µModules suit use as providers of core voltage to large FPGAs; the devices also have noise performance that is within the range of the on-chip SERDES (serializer/deserializer) functions that the FPGAs require. "Linear is the only supplier that has demonstrated that it can produce such modules with very high reliability," says Odabaee, claiming essentially zero failures for the series. The modules target designers who lack the expertise to build compact regulator functions themselves.

> A power-good output signal tracks the margining to indicate when the output is within limits.

Linear fabricates its own power MOSFETs for the µModules but says it has no intention of making these MOSFETs available separately: "The economics [of supplying] the MOSFET market are different from those of the specialist-linear-IC market," Odabaee says. Linear builds the FETs for low on-resistance and low gate charge and with a voltage rating tailored for each µModule. The LTM4608 operates at −40 to +85°C and costs $11.30 (1000). It brings the number of µModules to eight, and Linear plans to extend the series in four categories: high input voltage and high power, low input voltage and low power, very-high voltage and low to medium power, and buck-boost devices that transparently switch from step-down to step-up as the input voltage falls through the level of the regulated output.

—by Graham Prophet

▷**Linear Technology**, www.linear.com.

FIVE YEARS TO COMMERCIALIZATION FOR SILICON-NANO RESEARCH INTO LITHIUM-ION BATTERIES?

In general, you have two options with lithium-ion-battery technology. You can optimize the battery chemistry for high-energy storage in the kind of batteries you find in today's laptops and cell phones. These lithium-ion cells rely on cobalt cathodes, which have an unfortunate although rarely experienced ability to go into a thermal-runaway condition and catch fire. Or, you can optimize for power–that is, the ability to charge and discharge rapidly. GM (General Motors) is pursuing these batteries for its extended-range electric car, the Chevy Volt, which uses lithium-iron-phosphate batteries from A123 (a123systems.com), LG Chem (www.lgchem.com), and others. It's almost impossible to get a lithium-iron-phosphate battery to go into thermal runaway, but the trade-off is much lower energy storage.

After research into these problems, Yi Cui, assistant professor of materials science and engineering at Stanford University (www.stanford.edu), recently announced success in expanding the energy-storage capacity of lithium-ion batteries by using silicon nanowires for the anode; current batteries typically employ conventional carbon material for the anode. Silicon has a much higher energy capacity than carbon. However, silicon absorbs positively charged lithium atoms during charging and swells and then shrinks during discharge, resulting in cracks. Cui's research shows that, although the silicon nanowires still expand and contract, they don't fracture. Use of silicon nanowires results in a tenfold increase in energy storage, with the potential to last for more than 1000 cycles. (Actual laboratory cycles are currently in the tens, rather than thousands, of cycles.)

In an interview, Cui said that his research could within five years transfer the lithium-iron-phosphate-battery chemistry into a commercial product for A123 and LG Chem. To read the interview, go to www.gm-volt.com/2007/12/21/gm-voltcom-interview-with-dr-cui-inventor-of-silicon-nanowire-lithium-ion-battery-breakthrough.

—by Margery Conner

▶**General Motors Corp, www.gm.com.**

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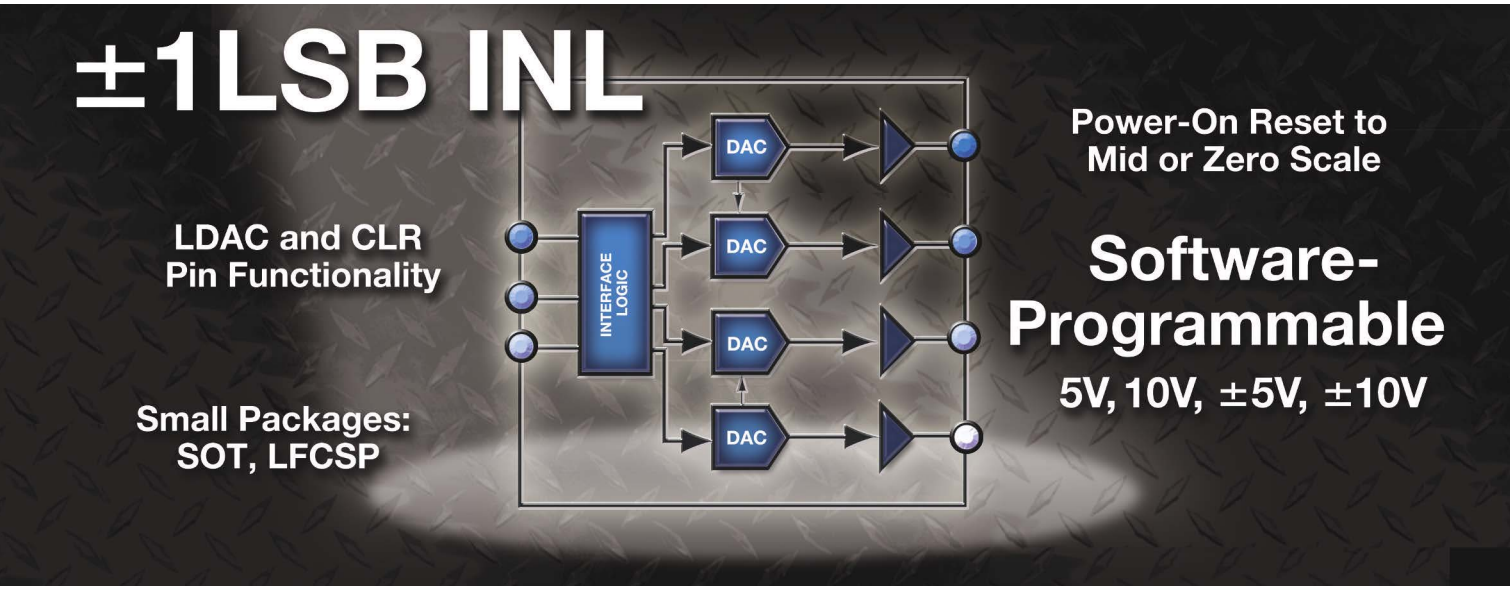

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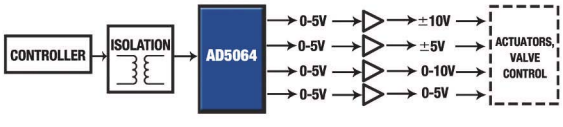

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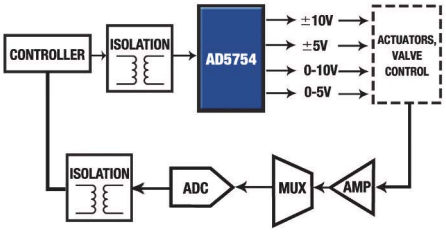

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VOICES

Green Hills Software's David Kleidermacher

David Kleidermacher is the chief technology officer at Green Hills Software, a company that provides high-performance compilers, software-development tools, and real-time operating systems for developers of embedded systems. Recently, during the Green Hills embedded-software summit, he answered a few questions about the two main topics of discussion at the summit: security and virtualization. The following is an excerpt of the interview. For the complete version, go to www.edn.com/080124p1.

What are the top challenges your company is focusing on to try to help your customers with their design efforts?

A Security is a top concern: How can we provide tools that help our customers address security—not merely from an operating-system perspective, but also from a position of addressing the whole picture? It's not just operating systems but all the things we need to do. We need to do a lot more on a lot of different planes to help people make the software more secure. We have shown that we know how to make our own software secure, but we have not yet fully enabled our customers to make their own software fully secure. From my perspective, it's a multitiered approach; operating systems and virtualization are definitely important, but you need the right runtime environment, the right software-development tools, and the right process—something we have not talked about much to date. You can talk about formal methods, but there is more to it than that, so that you can address how you go about developing your software so it is more secure and still meets the same time-to-market demands that you have.

Most applications cannot afford $1000 per line of code to ensure the same level of reliability as the space shuttle; the reality is that most of the software in the world does not need to be at that level. If you have a computer system running Windows, Linux, and application code, it might have 100 to 200 million lines of code running on it. How much of that code is high assurance? Only about 20,000 to 30,000 lines of code of that—say, the kernel and a couple of other special components—need to be fully secure.

The things we've learned about making our own software secure are streaming out in bits and pieces into our product base, but there is room for a lot more, such as in the automated-testing area, coding-standards enforcement, and tools that help you more reliably develop software. There are also the process things, and this area is one we have not historically been pushing much at all, but we are starting to touch more on it now.

"Virtualization" is a term that the industry is using across multiple contexts, such as design-time and runtime virtualization. Should the industry be using a single term to describe an abstraction concept to apply to multiple contexts?

A The term "virtualization," when you use it as an abstraction of anything, is too general. I have been pushing to use different terms to distinguish between the contexts because using a single term for all of them is confusing. Design-time virtualizations often refer to hardware-, software-, and co-prototyping tools that act as development platforms before the hardware is ready to support parallel development and shorter design cycles. I have proposed using the term "virtual prototype" to refer to these types of abstractions, and it may even be appropriate to have different terms for each of these types of prototypes. For runtime-virtualization tools, I like to use the term "virtual machine," or "virtual-machine monitor," or even "hypervisor" to apply to runtime virtualization, especially because no one has previously used these terms, especially "hypervisor," to refer to virtual-prototype contexts.

There is another classification that I use that takes it another step further—beyond design or runtime—to classify the general application areas it is for, such as virtual IT, which is concerned with consolidation and aggregation for better server management or even the flexibility to run different operating systems or hardware platforms. Another category is what I call virtual hybrids, which use virtualization as a tool to enable more flexible computing models. This [approach] is basically a runtime virtualization, but it is not just for the sake of virtualization, as virtual IT is pure virtualization. Virtual hybrids can [involve] running some legacy code alongside some real-time application or some security-critical application. A whole gamut of applications exists, and I think these types of applications deserve their own category because they are so different from your typical VMware or parallel-processing applications.

Compilers provide an important level of abstraction that enables them to optimize instruction sequencing; is anything preventing compiler technology from addressing systems as they continue to expand the amount of integrated and specialized resources and the number of connected processors in a single system?

A The compiler is starting do some things to accommodate this [scenario], but the current coding languages hamstring compilers today, partly because they do not automatically capture concurrency or the impacts of latency and bottlenecks in memory or special processing resources.

—by Robert Cravotta

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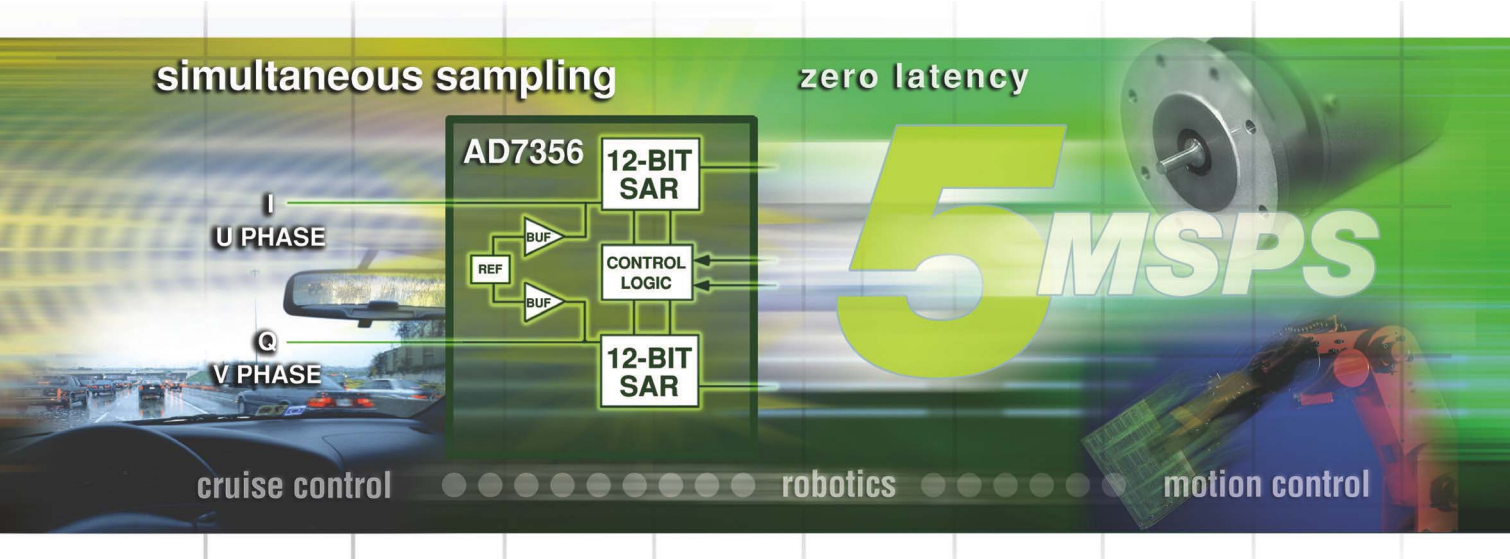

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ANALOG DEVICES

BY BONNIE BAKER

Delta-sigma ADCs in a nutshell, part 2: the modulator

A delta-sigma converter uses many samples from the modulator to produce a stream of 1-bit codes. The delta-sigma ADC accomplishes this task by using an input-signal quantizer running at a high sample rate. Like all quantizers, the delta-sigma modulator takes an input and produces a stream of digital values that represents the voltage of the input. You can look at the delta-sigma modulator in the time or in the frequency domain. If you look at a time-domain representation, you can see the mechanics of a first-order modulator (**Figure 1**).

The modulator measures the difference between the analog-input signal and the analog output of a feedback DAC. An integrator then measures the analog-voltage output of the summing junction and presents a sloping signal to the 1-bit ADC. The 1-bit ADC converts the integrator's output signal to a digital one or zero. Using the system clock, the ADC sends the 1-bit digital signal to the modulator's output, as well as back through the feedback loop, where a 1-bit DAC is waiting.

The 1-bit ADC digitizes the signal to a coarse output code that has the quantization noise (e_i) of the converter. The modulator output is equal to the input plus the quantization noise, ($e_i - e_{i-1}$). As this formula shows, the quantization noise is the difference of the current error (e_i) minus the previous error (e_{i-1}) of the modulator. The time-domain output signal is a pulse-wave representation of the input signal at the sampling frequency, f_S. If you average the output-pulse train, it equals the value of the input signal.

The frequency-domain diagram tells a different story (**Figure 2**). The time-domain output pulses in the frequency domain appear as the input signal (or spur) and shaped noise. The noise characteristic in **Figure 2** is the key to the modulator's frequency operation.

Unlike most quantizers, the delta-sigma modulator includes an integrator that shapes the quantization noise. The noise spectrum at the modulator output is not flat. More important, in a frequency analysis, you can see how the modulator shapes the noise to higher frequencies, facilitating the production of a higher resolution result.

The modulator output in **Figure 2** shows that the quantization noise of the modulator starts low at 0 Hz, rises rapidly, and then levels off at a maximum value at the modulator sampling frequency.

Integrating twice with a second-order modulator, instead of just once, is a great way to minimize low-frequency quantization noise. Most delta-sigma modulators are of a higher order. For instance, the designs of the more popular delta-sigma converters include second-, third-, fourth-, fifth, or sixth-order modulators. Multi-order modulators shape the quantization noise even harder to higher frequencies. **EDN**

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2. Baker, RJ, *CMOS mixed-signal circuit design*, Wiley & Sons, ISBN 0471227544, May 2002.

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.

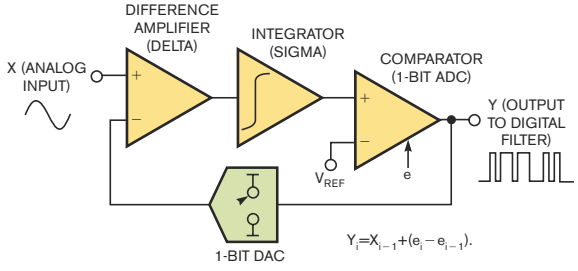

Figure 1 A time-domain representation shows the mechanics of a first-order modulator.

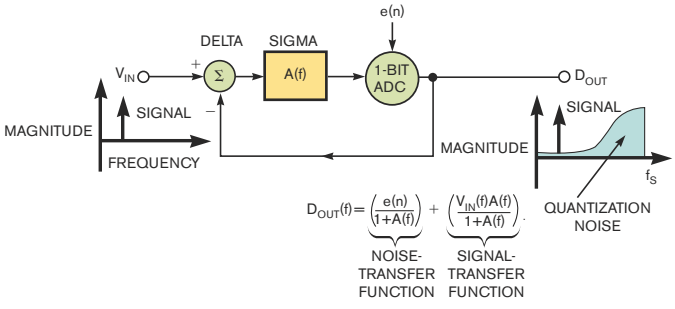

Figure 2 In a frequency-domain representation, the noise characteristic is key to the modulator's frequency operation.

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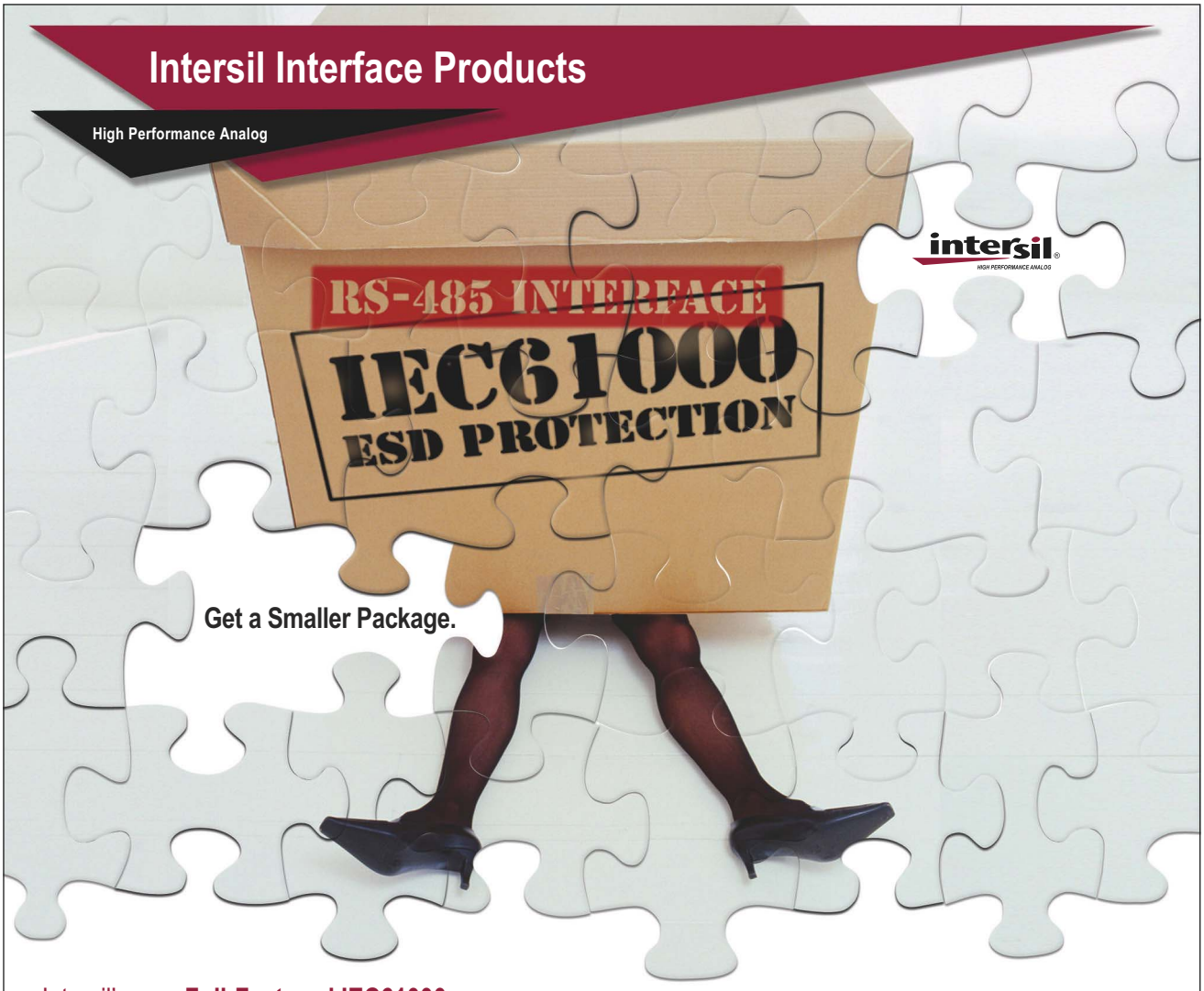

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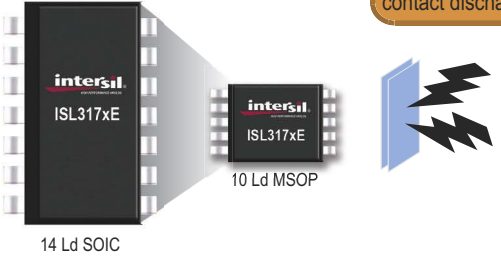

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ISL3172E	0.25	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3173E	0.5	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3174E	0.5	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3175E	0.5	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3176E	20	No	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3177E	20	No	No	8 Ld MSOP, 8 Ld SOIC
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The Dimage X50 digital camera

The Dimage X50 digital camera is a recent model in Konica Minolta's Dimage X series. The X60 is identical except for the lack of a view finder and a larger LCD. The utility of a view finder became apparent in this model after the magnetic latch on the Minolta factory case cracked the LCD. The view finder allowed you to use the camera until you could find a parts camera on eBay for $32.

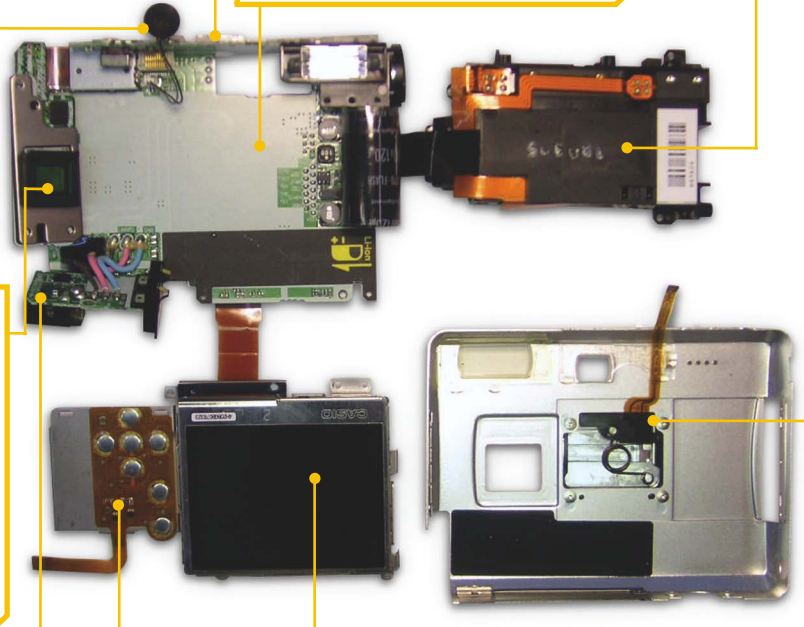
Like autos and most other consumer appliances, this camera is obviously designed from the outside in. A stylist designed the case; mechanical engineers made all kinds of boards, panels, and injection moldings. Then, the electrical engineers had to fit things onto the boards. It would be interesting to see Minolta redesign the camera from an electrical engineer's perspective, with all the electronics on one board and the developers designing buttons, microphones, and speakers to support this simplification.

The flash board plugs into the main board and holds pushbuttons on the top of the case. It carries a small lithium button cell to power the date and clock functions and to maintain the settings even during a battery change.

The main board holds the bulk of the electronics. Most of the components are on the underside, which is covered with a white silk-screen to protect the device from shorting against the optical-lens assembly. Several inductors and power components are on this side of the board.

A ribbon cable that carries signals for two focus motors and two position-flag sensors connects the 3× optical-zoom-lens assembly. Four terminals on the two focus motors indicate that they are stepper-type motors. In addition, there are four circuits for an aperture motor. The view finder assembly (not shown) screws to the top of this unit—a combination of plastic and metal sheets as well as several metal rods on which the lenses slide.

The microphone plugs into the main board and resides in a pocket molded in a complex plastic carrier.



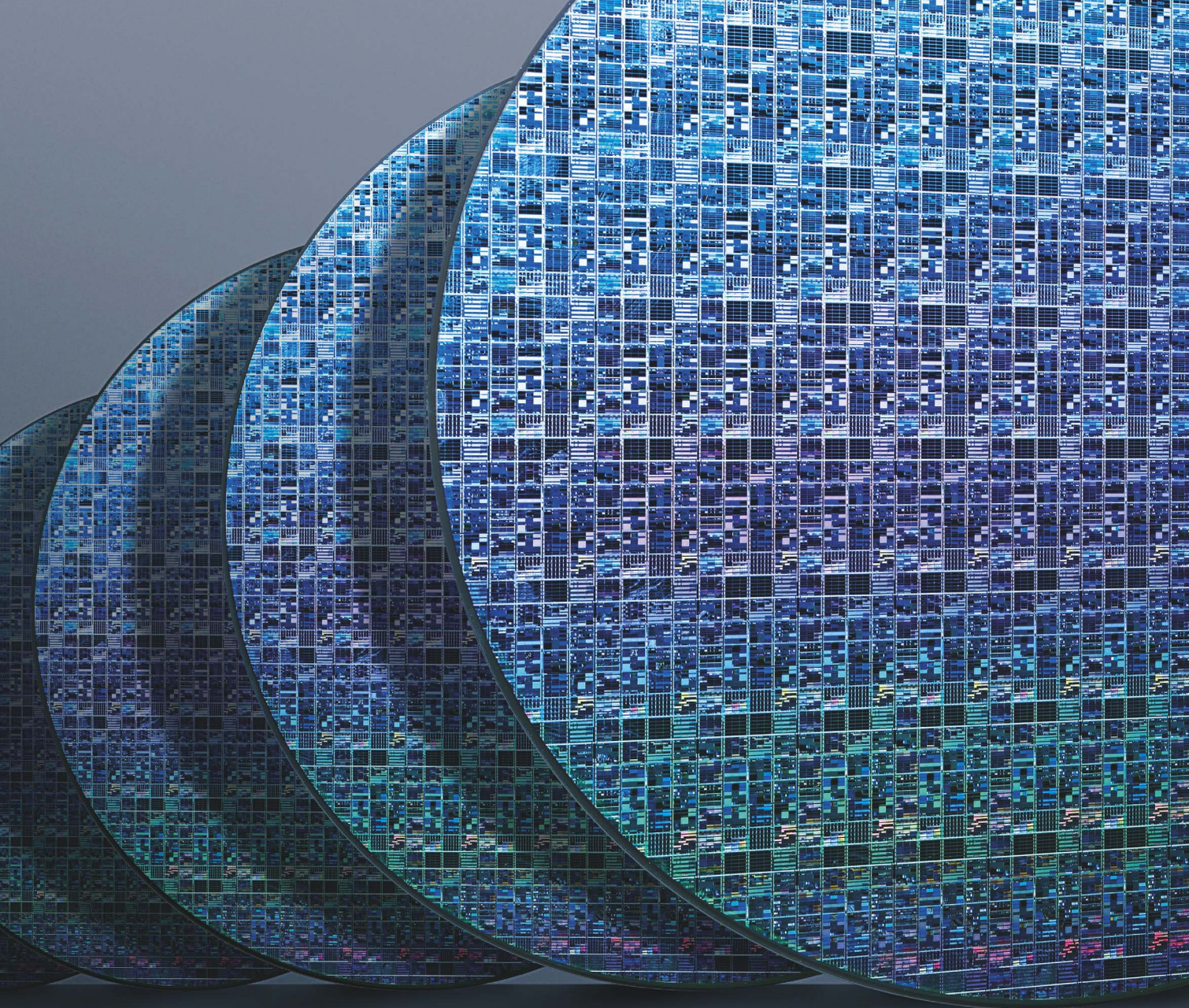
The front cover carries a slide switch that connects to the main board with a ribbon cable, providing one of the camera's most endearing functions: You don't have to poke a tiny button to turn the camera on; just slide the 1×2-in. cover off the lens, and the camera is ready. There are two clear acrylic windows in the cover—one for the flash and one for the view finder. The black area is tape that prevents shorting the battery to the metal case.

The CCD board, with a metal mounting plate that ensures its location precisely in the optical path, plugs into the main board. It includes a short ribbon cable to a board, which holds the interface connector that plugs into the main board.

Pigtail connectors attach the battery-terminal board to the main board. The terminal board also carries the external dc-power connector. The terminals are inside a plastic housing that fits into the plastic carrier in the camera.

Rear-panel pushbuttons mount on the LCD metal-panel assembly. The stiffness of the metal panel improves the snap-action feel of the buttons.

The LCD mounts on a metal panel that straddles the components on the underside of the main board. The panel itself has a metal back, which is useful to prevent EMI (electromagnetic interference) from radiating through the LCD glass. The ribbon cable uses the same differential signaling as notebook-computer-LCD screens.



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BY JIM SYLIVANT • ENGINEERING CONSULTANT

Blown fuse has a meltdown

DANIEL VASCONCELLOS

In midcareer, I became a component engineer. Soon after I arrived in my new department, I faced a problem that had been ongoing for some time. It seems that a simple fuse in a CRT display had been having high failure rates. My new department had thoroughly tested samples against its specifications. A previous test engineer had designed a test fixture so that he could test batches of this fuse for all spec items. The specification required the fuse to open at a certain percentage over its nominal rating within a certain number of milliseconds over a range of temperatures, as well as after shock and vibrations. The previous engineer had done a splendid job of testing to verify that the fuse met all specifications.

However, in the application, high failure rates continued. My first step was to measure actual current in the application to ensure that we had chosen the proper fuse. I found that, besides a small, brief start-up current, the nominal value quickly settled to values well within the fuse's rating. I didn't suspect the brief start-up surge of causing a problem. After going over previous test results and in-application testing, I could find no explanation for the high failure rate. In desperation, I sent some samples to our on-site materials lab and asked the folks there to measure the cross-section diameter of the fuse element and identify the alloy used. Fortunately, the lab assigned the job to a very competent materials engineer who went the extra mile by analyzing the fuse after subjecting it to brief current pulses. In a few days, I got back beautiful microphotographs showing an unexpected construction technique. The photos showed that, instead of using a single alloy of some low-melting-point metal, the element consisted of three types of metal. It had a large, circular, tungsten inner core. Over the tungsten was a thin plating of copper; yet another thin layer of silver lay over the copper. Even more surprising were the photos the engineer took after subjecting the fuse to brief overcurrents. He found that, by charging a capacitor to various voltages and discharging it by short-circuiting it with the fuse, he could create a controlled amount of surge current. The photos showed that, after some surges, the silver layer reached its melting point, causing it to liquefy. After more surges, the silver completely melted away, leaving only the tungsten core with its thin copper plating. Because silver has such high electrical conductivity, virtually all the current from the surges initially flowed entirely through the outer silver layer. Afterward, additional surges flowed mostly through the thin copper layer because copper has higher conductivity than tungsten. That layer eventually melted. Now, only the tungsten core with its high resistance remained. With more surges, all current now had to flow through the remaining tungsten core. As more surges occurred, the tungsten heated up enough to gradually grow thinner and finally disintegrate.

We then realized that this trilayer-construction technique gave the fuse the ability to "remember" the accumulation of brief overload-current surges. Each surge at power-on contributed to small changes that eventually caused the fuse to open. Steady-state testing had not revealed this characteristic. As a result of its trilayer construction and the metals used, the fuse had memory. The solution was to change to a conventional fuse with a single element of low-melting-point alloy—that is, one that did not possess memory. This realization was the beginning of many such discoveries—that you can diagnose most problems by going back to an understanding of the basics. EDN

Jim Sylivant is an engineering consultant and lives in Apex, NC. Like Jim, you can share your Tales from the Cube and receive $200. Contact Maury Wright at mgwright@edn.com.

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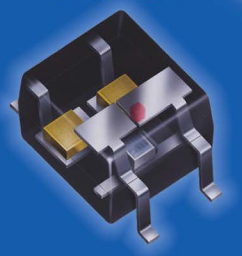

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Using Clock Conditioners to Clean Recovered Clocks

Application Note AN-1734

Dean Banerjee, Applications Engineer

Introduction

In wired communications, there is a need to recover a clock from the data. Having the clock encoded in the data eliminates the need for a wire to transmit the clock, and also helps with skew issues. This application note investigates the impact of cleaning the clock at every stage, as well as at the end.

Serializer-Deserializer (SerDes) parts such as the SCAN25100 can take a set of parallel data and convert it into a series set of data that can be sent on a single wire. Another SerDes part at the receiving end can be used to generate the parallel data from the received series data. This is a very effective technique for sending data over long distances, but the recovered clock will have added phase noise (jitter) relative to the original clock used to generate this serial data.

When data is transmitted over long cables, the signal will become weaker and the Signal-to-Noise Ratio (SNR) will be less. If the length of cable is too long, it will not be possible to recover the clock. For this reason, a SerDes part can be used as a repeater, where it receives the serial data, recovers the clock, and then re-clocks the data using the recovered clock or a jitter-cleaned clock. In this way, data can be transmitted over much longer distances.

Clock conditioners, such as the LMK03000C, can be used to take this dirty (higher phase noise/jitter) clock and generate a clean clock (lower phase noise/jitter) that is the exact same frequency.

Jitter Calculation

Phase noise is more descriptive than jitter. Jitter can be calculated from phase noise, but not the other way around. Given a phase noise profile, carrier frequency, and lower and upper limits for integration, the jitter can be calculated as follows:

$$Jitter = \frac{\sqrt{\int_{LowerLimit}^{UpperLimit} 10^{PhaseNoise(Offset)/10} \cdot dOffset}}{2 \cdot \pi \cdot Frequency}$$

From this formula it is apparent that minimizing jitter is a matter of minimizing the area under the phase noise curve.

Choosing the Optimal Loop Bandwidth

The loop filter can be implemented with one external resistor and two external capacitors. These components can be chosen to adjust the loop bandwidth of the system. At frequencies below the loop bandwidth, noise from the 30.72 MHz recovered clock pass through, but the Voltage-Controlled Oscillator (VCO) noise is attenuated. At frequencies above the loop bandwidth, the noise of the 30.72 MHz recovered clock is attenuated, but the VCO noise passes through. Therefore, the optimal design choice for the loop bandwidth depends on the noise of the VCO and recovered clock.

In this case, the VCO used was the internal VCO of the LMK03001C clock conditioner. The recovered clock was from the SCAN25100, and is shown for one hop, two hops, or three hops in ***Figure 1***. Normally, one finds the frequency at which the free-running VCO noise is equal to the other in-band noise sources and adds 25% to this in order to find the optimal jitter. However, in the case of dealing with recovered clocks, it makes sense to round this down a little bit, since the phase noise may vary with the number of hops and data.

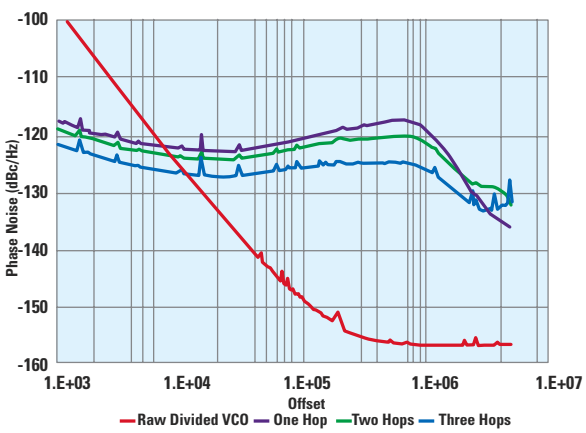

Figure 1. Determining which Loop Bandwidth to Use

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Implementation

In order to show all these techniques, three hops with the SCAN25100 were used and the final stage was cleaned with the LMK03001C clock conditioner. From *Figure 1*, we see that the optimal loop bandwidth for three hops is about 7.2 kHz. However, the choice of three hops is arbitrary, and perhaps more hops could be used.

For this reason, a narrower loop bandwidth of 4 kHz was used to be sure that this solution would be robust if more hops were used.

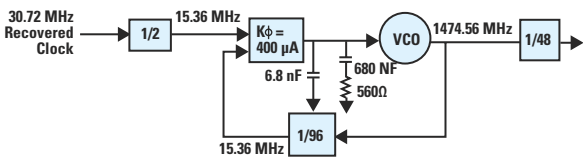

Figure 2. LMK03001C Setup for Cleaning a 30.72 MHz Recovered Clock

Note that in *Figure 3*, the recovered clock has lower jitter. If one uses an integration limit of 100 Hz to 5 MHz, then the recovered clock has a jitter of 5.3 ps and the cleaned recovered clock has a jitter of 1.4 ps.

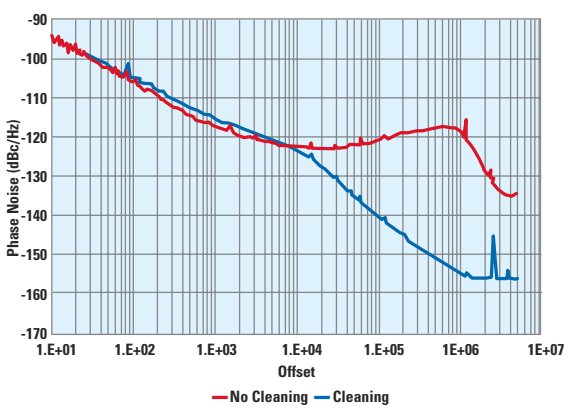

Figure 3. LMK03001C Setup for Cleaning a 30.72 MHz Recovered Clock

Note that in the range of 100 Hz to about 8 kHz, the clock conditioner actually adds a little phase noise. This is because the VCO noise is contributing here. If this is a major concern, the loop bandwidth should be increased. This design was done with a wider loop bandwidth as well and the jitter was reduced to around 900 fs.

Conclusion

The SCAN25100 and LMK03001C families are an excellent choice for sending and recovering data. In a multi-hop architecture, the SCAN25100 has a built-in reference clock that makes it such that there is no reference clock necessary for any of the SCAN25100 parts, except for the first in the series that is used to serialize the data.

The LMK03001C is an ideal choice for cleaning this clock, since it has excellent phase noise performance at higher offset frequencies. The noise of the reference clock of the SCAN25100 deteriorates primarily at higher phase noise offset frequencies when increasing the number of hops. So filtering at every hop, as opposed to just the last hop, only gives a marginal benefit to jitter cleaning, since this noise will all be filtered at the last hop. However, there could be reason to clean the clock at every hop if there was a need to use this recovered clock at every hop, instead of just at the very end.

The LMK02000 clock conditioner allows the user to supply a VCXO in order to obtain improved phase noise performance close to the carrier, if that is required for system reasons other than data clocking. ■

For a more detailed version of this article, including information on recovered clocks, visit:

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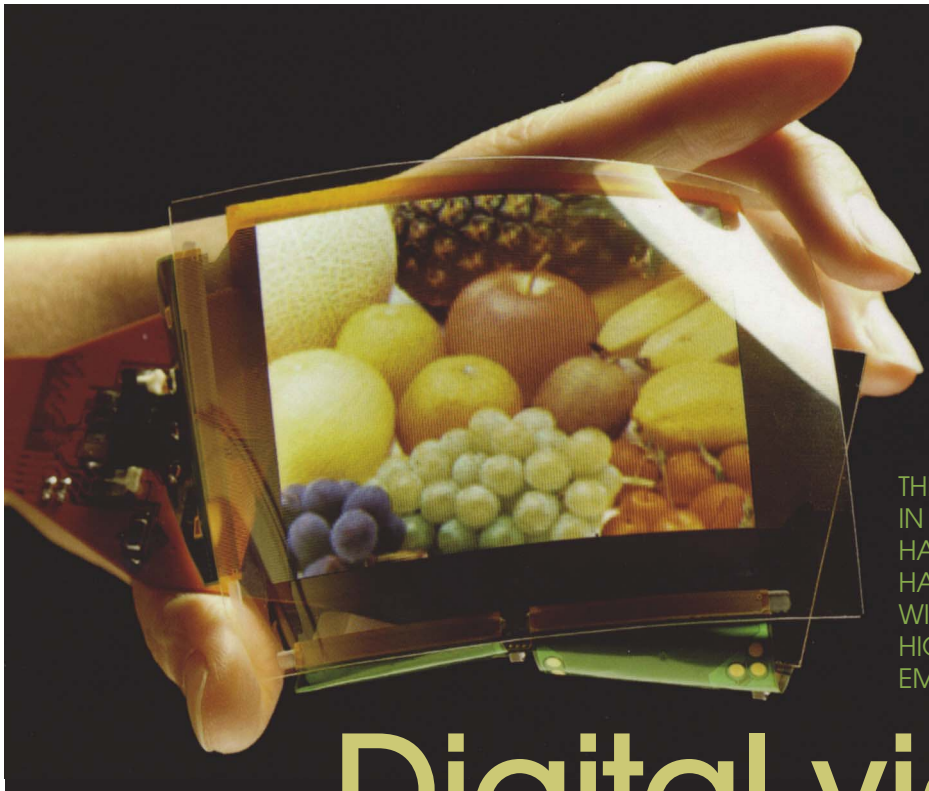

Figure 1 Sony is producing a lightweight and flexible full-color display by depositing an organic TFT directly onto a plastic substrate.

THE VIDEO REVOLUTION IN CONSUMER DEVICES HAS PRODUCED LOWER HARDWARE COSTS ALONG WITH EXPECTATIONS FOR HIGHER PERFORMANCE EMBEDDED DESIGNS.

Digital video PUSHES THE EMBEDDED-TECHNOLOGY ENVELOPE

BY WARREN WEBB • TECHNICAL EDITOR

For years, video has been an integral part of specialized industrial systems, such as surveillance and factory inspection. However, it has only recently become a viable addition to a range of embedded products. Specifically, the proliferation of image-capture and -playback features in high-volume consumer electronics, such as mobile phones, has produced an abundance of low-cost hardware and software tools to simplify digital-video integration. This widespread availability of digital video in consumer devices has also raised the expectations of embedded-system customers who are no longer content with a user interface that simply displays static information. Users want the same performance from an embedded system as they get from a desktop computer or even a low-cost portable video player. Unfortunately, designers must pay a price to join the digital-video revolution. Designers may have to expand built-in storage, increase processor power, redefine the networking bandwidth, re-evaluate display characteristics, and possibly upgrade the real-time performance of potential products.

Although most consumer-device videos are strictly for entertainment, a multimedia presentation in an embedded device can serve a number of functions. For example, a video display may spice up a mundane product or simplify an overly complex device. Designers can use digital video to differentiate products from the competition and create a unique theme for an entire product line. A video- or graphics-based user interface, along with a network connection, allows remote software upgrades and functional modifications. Built-in training and troubleshooting videos may eliminate or reduce initial installation costs and service calls. With high-bandwidth streaming-video features, customer-support personnel can also interact in real time with customers to solve operational problems or isolate defects.

There are many variations of digital video, and the right choice depends on the system resources, networking capabilities, and operational modes of the embedded device. Obviously, the data volume and bandwidth required to drive a high-definition television are orders of magnitude higher than those necessary to activate a mobile phone's 128×160-pixel screen. Most digital-video strategies will impose new hardware and software requirements on the embedded system. An operating system with real-time capability, built-in multimedia features, and device drivers will save on development time. In most cases, you must compress video data for transmission over a communications channel or for local storage. A high-speed networking connection to the Internet or local servers is necessary to stream remote video data in real time.

DATA SQUEEZE

One of the earliest design considerations in any embedded-video-system design is to provide the computing resources necessary to run compression and decompression algorithms or codecs. For example, a typical uncompressed television-video stream requires a data rate of more than 20 Mbytes/sec and more than 36 Gbytes to store a half-hour segment. Depending on the algorithm in use and the image content, video compression can reduce bandwidth and storage requirements by a ratio of approximately 30-to-1. Typical compression algorithms for video work by dividing the image into small blocks and then transforming each block into a frequency-domain representation. After transmission or storage, an inverse-cosine transform returns the frequency coefficients to the 8×8-pixel image block. Similar in processing requirements, both the forward- and the inverse-cosine transforms require only a few hundred instruction cycles on a typical DSP. Two principal organizations define and maintain today's popular image- and video-compression standards. The ITU (International Telecommunications Union) specializes in telecommunication applications and supports the H.26x standards for video telephony. The ISO (International Organization for Standardization) focuses on consumer applications, such as MPEG standards for video.

AT A GLANCE

- Video features in high-volume gadgets give embedded-system designers a new set of low-cost development tools and silicon signal processors.
- Digital video requires complex compression strategies to live within the limited bandwidth and storage limitations of embedded devices.
- Digital-rights-management software may be necessary to process and display copyrighted digital data.
- Embedded systems with digital video heighten complexity with 32-bit processors, real-time operating systems, and megabytes of memory.

In addition to codecs, media-centric embedded systems may include DRM (digital-rights-management) software to process some copyrighted material. DRM schemes attempt to enforce copyright or other usage restrictions that the copyright owner defines. For example, DRM may limit where, when, or the number of times that a user can reproduce material. The compressed-data side of the encoder or decoder uses DRM where the data rates are lower. Although details are usually secret, most DRM algorithms are less complex and easier to implement than the codec. The Microsoft Vista operating system contains the PVP (protected-video-path) system that can prevent DRM-restricted content from playing while unsigned software is running. PVP can also encrypt information during transmission to the monitor or the graphics card, which makes it more difficult to make unauthorized recordings.

Figure 2 The NI 1742 smart camera includes an image sensor, a processor, and vision-analysis software to return inspection results instead of images.

The display screen is the focal point for any embedded-video system, and designers base most of today's products on active-matrix LCD (liquid-crystal-display) screens or the more recent OLED (organic-light-emitting-diode) technology. LCD screens are currently the most popular because of their low power requirements, reduced weight, image quality, response time, and reliability. LCDs consist of cells of a light-polarizing liquid sandwiched between two perpendicularly polarized glass panels driven by a matrix of TFTs (thin-film transistors). An electric current changes the polarization characteristics of the liquid and blocks light transmission though that cell. OLED displays are gaining popularity in embedded-system applications because the technology offers potentially brighter, higher contrast images with less power and lower manufacturing costs. These displays rely on organic compounds that a multilayer-printing process deposits in rows and columns onto a flat carrier. Unlike the traditional LCD, OLED displays require no backlight, and they offer a much faster response. One possible drawback of OLED displays is the reduced lifetime of certain color organic materials. Sony recently unveiled a flexible, full-color OLED display that it based on organic-TFT technology (**Figure 1**). OLEDs typically use a glass substrate, but Sony developed new technology for depositing organic TFT directly onto a plastic substrate, producing a thin, lightweight, and flexible full-color display. The 2.5-in., 0.3-mm-thick prototype display supports 16.8 million colors at a 120×160-pixel resolution.

SMART CLICKS

Automated-inspection applications, such as part location, package inspection, and assembly verification, typically require significant video processing to analyze real-time images. To simplify this process, National Instruments recently introduced the NI 1722 and NI 1742 smart cameras, which com-

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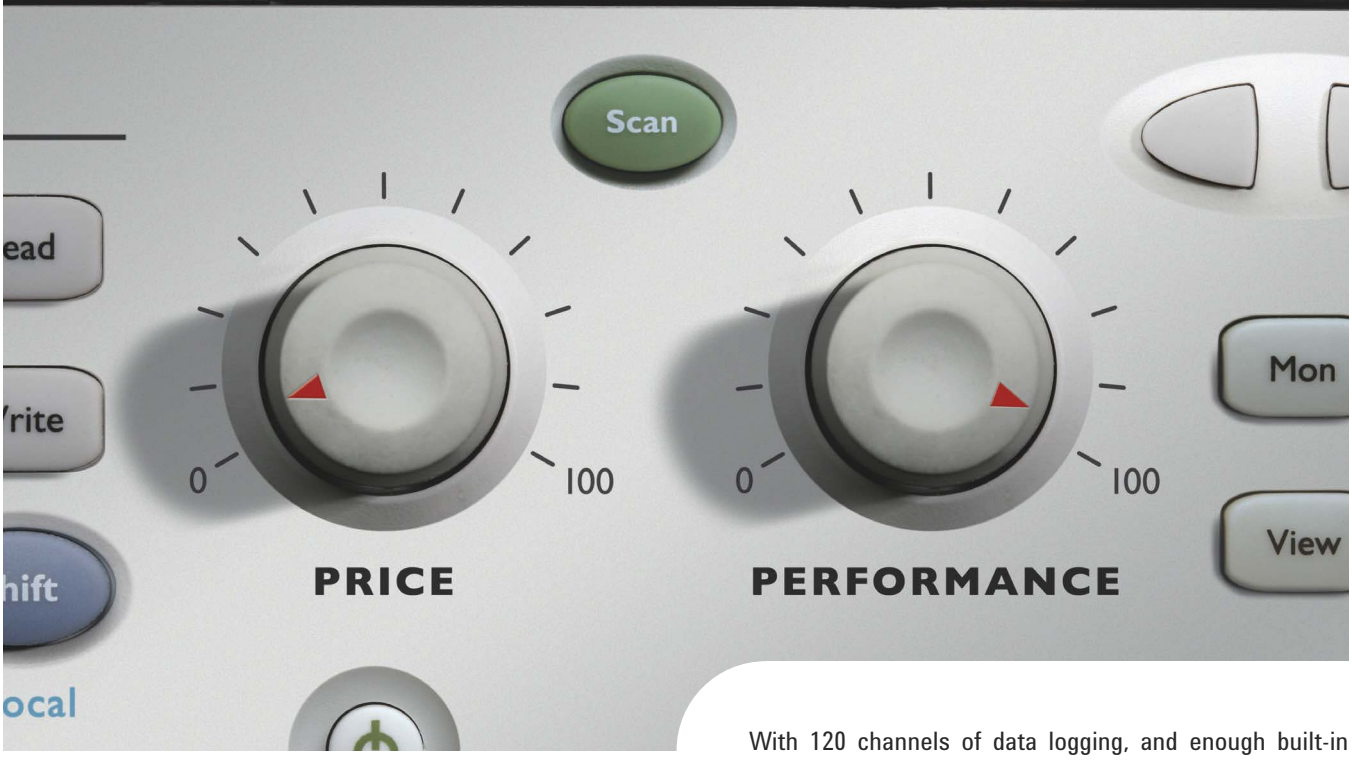

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bine an industrial controller, an image sensor, and vision-analysis software to return inspection results instead of images (**Figure 2**). NI ships the cameras with its Vision Builder software, a menu-driven environment for configuring and deploying machine-vision applications without programming. For more advanced applications, the cameras are compatible with the full LabView library of image-processing and machine-vision algorithms, such as edge detection, pattern matching, and optical character recognition. The NI 1722 features a 400-MHz PowerPC processor, and the NI 1742 includes the 533-MHz version. Both cameras feature a monochrome, 640×480-pixel Sony charge-coupled image sensor plus built-in I/O. This I/O includes two optoisolated digital inputs, two optoisolated digital outputs, one RS-232 serial port, and two GbE (Gigabit Ethernet) ports with support for industrial protocols, including Modbus TCP (Transmission Control Protocol). In addition, the NI 1742 includes quadrature-encoder support and built-in LED-lighting drive, which provides as much as 500-mA constant current and 1A strobed current. The NI 1722 and NI 1742 smart cameras cost $1999 and $2499, respectively.

With support for today's mobile arsenal requiring as many as 70 formats, content providers are turning to transcoders to translate between the various video configurations. Transcoding is the direct digital-to-digital conversion from one codec format to another to fit the target device. It involves decompressing the original data to a raw intermediate format and then re-encoding it into the target format. Texas Instruments now offers a new digital-media processor for video transcoding in media gateways, multipoint control units, and set-top boxes. The new DSP-based TMS320DM6467 DaVinci processor system on chip provides real-time, multiformat-video transcoding. Integrating an ARM926 core and 600-MHz C64x DSP core along with a video coprocessor, a conversion engine, and targeted video-port interfaces, the system claims a tenfold performance improvement over previous-generation transcoders. The TMS320DM6467 processor costs $35.95 (large volumes).

MORE AT EDN.COM

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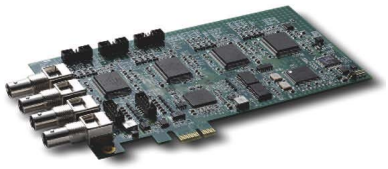

Figure 3 The PCIe-RTV24 high-speed video-capture card supports four channels of real-time image acquisition at frame rates reaching 30 frames/sec.

High-bandwidth machine-vision, security, and video-surveillance applications, such as position location, biometric face recognition, and vehicle-license-plate identification, start with data sampled directly from the content provider's signal source using analog-capture cards, or frame grabbers. Targeting these applications, Adlink Technology recently announced the PCIe-RTV24, a high-speed video-capture card featuring PCI Express technology and supporting four channels of real-time image acquisition at frame rates as high as 30 frames/sec (**Figure 3**). It accepts standard composite-color or monochrome-video formats, features programmable resolution, and generates bit maps in all popular digital formats. With RGB24, an RGB format with 24 bits/pixel, for example, the output includes an 8-bit pixel value for each of the red, green, and blue colors. The module also provides a watchdog function and offers four digital-I/O signals that you can use for strobe-light control, trigger acquisition, and alarm signals. The PCIe-RTV24 supports Microsoft Windows or Linux and costs $195.

REMOTE VIDEO

Although video features have many benefits for new-product design, the required development budget plus recurring display and signal-processing resources may be too costly for some deeply embedded devices. These projects can still take advantage of digital video by employing a removable user interface that may be a general-purpose device, such as a PC, PDA, or cell phone. A short-range communications link, such as Bluetooth, 802.11, infrared, or even a hard-wired connection, enables graphical interaction with much less development effort and minimal hardware cost. If the embedded device has a built-in networking connection to the Internet, you can also create a remote, video-based user interface that is accessible from any browser worldwide.

Digital video is now commonplace in high-volume consumer electronics and desktop computers, and embedded-system designers feel pressure from customers to emulate the user experience to remain competitive. Video instruction and real-time user interaction promise to replace more of the printed documentation with each new system generation. The transition to video will probably appear first in highly portable embedded devices using the low-cost technology from cell phones and video players. The growing supply of off-the-shelf hardware and software products gives embedded-system designers the tools to incorporate a sophisticated video interface into every system. Improvements in compression algorithms and the availability of high-volume silicon will continue to lower costs and make complex multimedia features easier to justify with each new product generation. EDN

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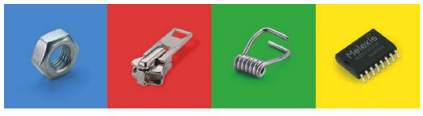

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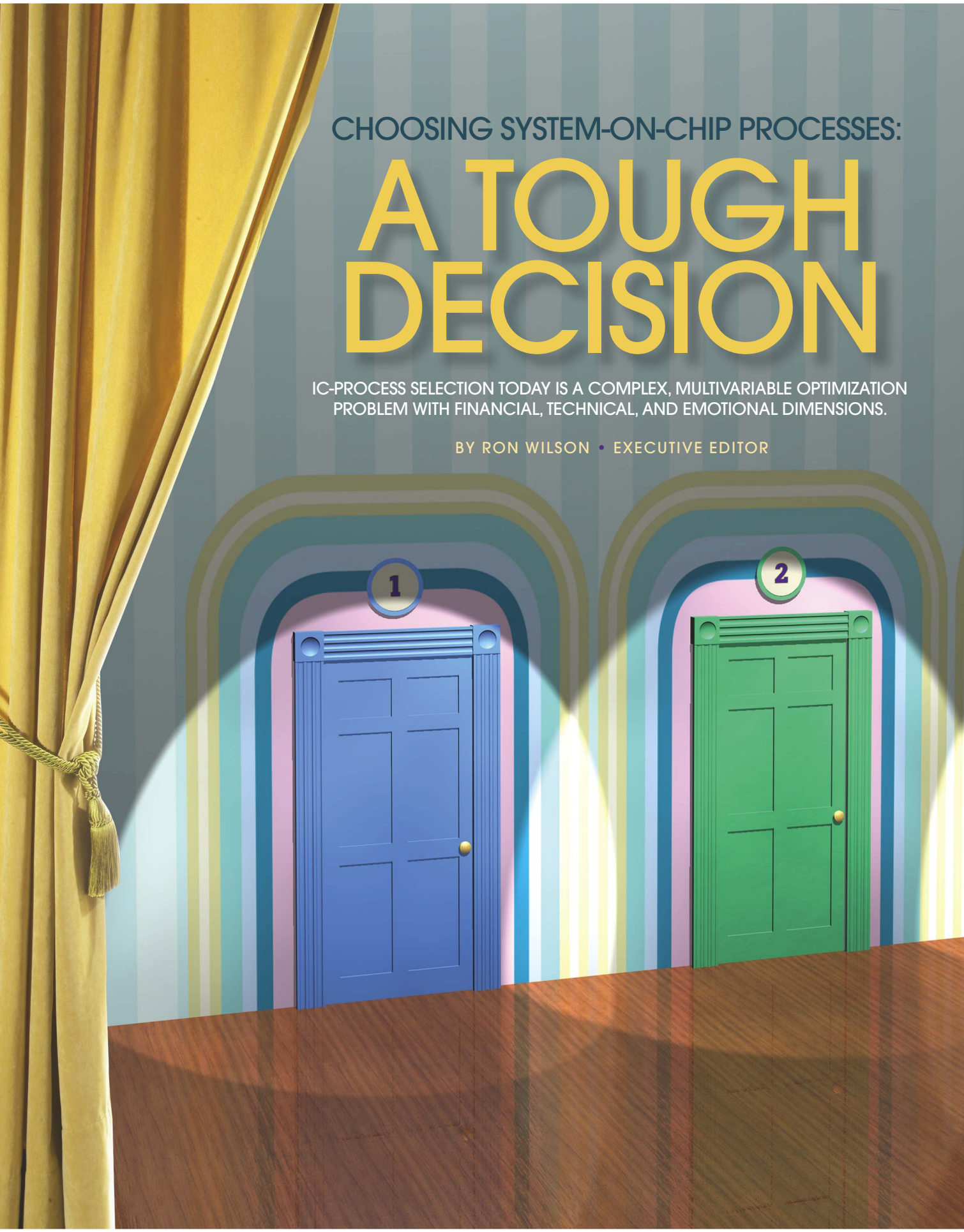

CHOOSING SYSTEM-ON-CHIP PROCESSES:

A TOUGH DECISION

IC-PROCESS SELECTION TODAY IS A COMPLEX, MULTIVARIABLE OPTIMIZATION PROBLEM WITH FINANCIAL, TECHNICAL, AND EMOTIONAL DIMENSIONS.

BY RON WILSON • EXECUTIVE EDITOR

An unwritten assumption of the chip-design profession is that it is always best to use the newest available process: best for your résumé, and best for the design. The most advanced process you can get will make the chip faster, lower power, and less expensive than that old "mature" process you used last year. Flaws in this reasoning have always existed, but the old rule is now breaking down on a grand scale. Far from assuming that they will use the latest and greatest, today's design teams find that process selection has in itself become an important early step in the design flow.

The causes for this change are easy to find. Diminishing returns have set in, at least for some kinds of structures, on both performance and die area. A given block in a 65-nm process is no longer automatically smaller and faster than it was at 90 nm. Power no longer decreases monotonically with process geometry. Actual energy consumption today is a complex brew of process, library, and design choices. Seasoning this mix are inscrutable end-user behaviors and a growing list of process variations. The result is often not the pudding the designers had in mind.

So, how are design teams choosing their target processes? A number of designer managers and service providers provided some answers. Despite a variety of environments and viewpoints, some patterns have emerged.

WHEN YOU HAVE NO CHOICE

The easiest case to discuss might appear trivial: The chip has a technical requirement that dictates a particular process choice. Examples include integrated RF at frequencies greater than 10 GHz; high-sensitivity, precision analog circuits with very high dynamic range; and circuits that must operate at high voltage. "High interface-voltage levels sometimes dictate a solution," says Bob Klosterboer, senior vice president for automotive and industrial applications at AMI Semiconductor. A specialist in mixed-signal and high-voltage ASICs, Klosterboer often sees these issues. "Sometimes, it is signal voltage, not interface level, that is the issue. Advanced processes use very low core voltages. But anything above a 10-bit dynamic range can be hard to achieve at even 1.8V."

Designers can, in principle, address these issues and others, such as the need for large amounts of integrated nonvolatile memory, by adding modules to a standard logic process. But that approach can quickly become expensive in NRE (nonrecurring-engineering) costs, design complexity, and yield. "RF designers may ask for

metal-insulator-metal capacitors, thick upper metal layers, and triple-well RF transistors," observes Ana Hunter, Samsung's vice president of technology. "But management may tell them to work with what they get in the standard digital process."

Another alternative is to use an SIP (system in package, **Figure 1**). Massively high-volume use of SIPs in cell-phone handsets has driven this technology to a level of maturity that makes it viable for even lower-volume applications, Klosterboer suggests. "Often, SIP is an alternative, but it sometimes doesn't get the consideration it should because design teams don't understand it well," he says.

Yet, special cases sharply narrow the process choice, and designers can't easily circumvent these scenarios. Two of these cases, Klosterboer points out, are high-temperature operation and extended product life—both facts of life in the automotive industry. "For example, chips that will go inside a transmission case may have to operate continuously at up to 150°C," he says. "But, in advanced processes, the dice may be rated for only 50 to 70°C. You may find a foundry process characterized at 125°C, but it then turns out that the libraries you want to use have been characterized only to 85°C. It's a problem." Extended life can also be an issue, requiring the design team to ensure that its process choice will still be around and running wafers in 10 years.

AT A GLANCE

- The most recent available process is no longer automatically the best choice.
- Specific needs constrain some process selections, but SIP (system-in-package) approaches can often address these needs.
- Finding the best process is a multidimensional optimization problem that involves lifetime costs, IP (intellectual-property) needs, design requirements, and analysis of risk.
- The whole team of design partners needs to be involved in the decision.

TOO MANY CHOICES

Beyond the cases in which process choice is mandatory lies the land of uncertainty: most chip designs in which many processes might be suitable. To settle on one, design teams go through a process of exploring, evaluating, and selecting. Hugh Durdan, vice president of marketing at eSilicon, lumps these considerations into about four categories. In rough order of priority, they are cost, IP (intellectual-property) maturity, technical requirements, and process maturity. "Each of these factors in isolation is straightforward," Durdan says. "The difficulty is in balancing between them."

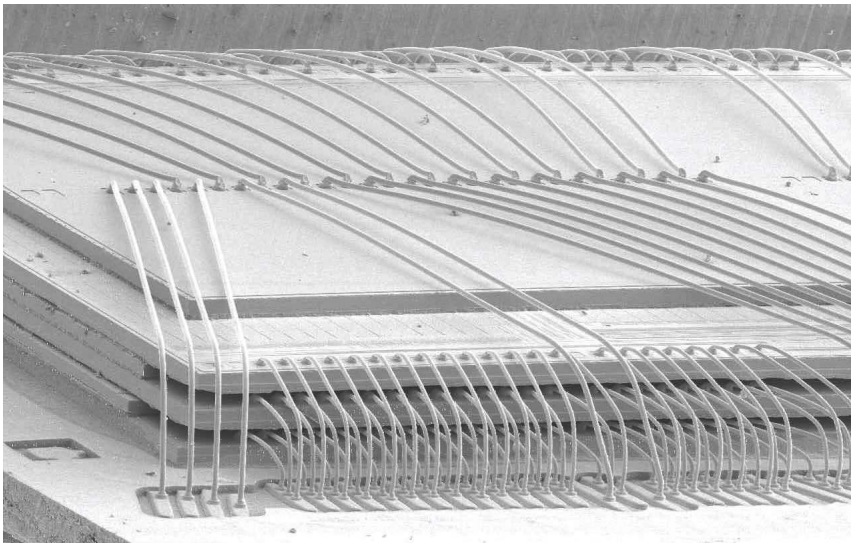

Figure 1 Complex, stacked-die systems in package have become business as usual for the packaging industry and represent an important approach to some process-selection problems for SOCs (courtesy Stats ChipPAC).

Perhaps the most obvious of these categories and, in some ways, the easiest to misunderstand, is cost. "The single factor for us is price; that pushes all the decisions," says Jose Calero, chief technology officer of powerline-networking-chip vendor DS2 (Design of Systems on Silicon). "But we look at the cost of the full solution, not just of the silicon." DS2 could be the poster child for consumer electronics. The company's designs are not performance-constrained and do not have unusual technical requirements. But they are nonetheless complex SOCs (systems on chips) with formidable analog content and digital-signal processing, and they aim for high-volume markets. This fact makes unit cost more important than NRE.

Calero says that DS2 starts its cost-estimation process with a detailed knowledge of the digital and analog blocks that will go into the new design, because the new chip will usually be an incremental change from an older one. The analog-device designers can start early with a prospective process' design kit and do their block designs through preliminary placement. The company then takes the gate counts for the digital blocks and the preliminary analog designs to prospective vendors for quotations. In general, the lowest quote wins.

COMPLEXITIES OF COST

Unit cost depends on die size. "In general, we are pretty good at estimating die size, given a good idea of the libraries the customer will use," says Paul Rousseau, account manager on emerging accounts at TSMC (Taiwan Semiconductor Manufacturing Co). The estimation is more than a matter of counting standard cells, because I/O, power routing, decoupling capacitors for the power routing, and passive components for analog circuits can all be major factors in the final answer. But foundries or experienced design partners can often base their estimates on completed designs with similar characteristics. Experience is vital to this estimation. "We've been using a technology internally before we make it available to customers," says Jonathan Stanley, senior account manager at Fujitsu. "So we often have prior experience with similar blocks, as well as internal estimation tools, to estimate die area." And die size isn't necessarily

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the only component of unit cost: There are also yield, test costs, and packaging to factor in. Any one of these items has the potential to cost more than the die.

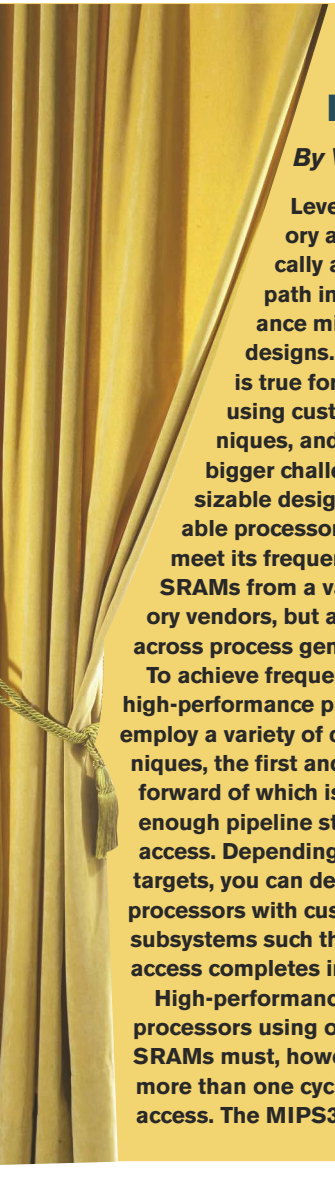
Another important unit-cost consideration is the opportunity to do a design reduction or a full redesign to bring down the silicon cost during a product's life. "Some people do their planning based on doing a simple die-shrink later," says Brad Paulsen, vice president of business development at TSMC. "They often use midstep processes that allow them to do a straight shrink and end up with a smaller die, rather than having to do a full redesign for a more advanced process node."

Unit cost is not the only cost consideration for most design teams, although it is for consumer-market products, such as DS2's. "When we hear people say, 'We can't afford to do a 65-nm design,' it raises flags," says TSMC's Paulsen.

"If you expect high volumes, the question is whether you can afford not to do 65 nm," TSMC's Rousseau adds.

If the expected unit volume is not that great, other factors intrude: NRE, IP-license and -royalty costs, personnel costs, and outsourced-contract costs are a few that Paulsen names. These factors can lead to trade-offs. "You can go for a smaller die at 90 nm and pay $1 million in tooling costs," says AMI Semiconductor's Klosterboer. "Or you can accept a larger die size at 350 nm and pay $30,000 in tooling. Volume is very important." Further, the design team has to decide on licensing IP, contracting with someone to design critical blocks, or doing the job in-house. Here, questions of capability and risk become part of the cost equation. "Often, we'll see start-ups that assume they are going to do all the design themselves," Paulsen says. "Sometimes, we have to counsel them that it just doesn't happen that way."

There is also a matter of design teams biting off more than they can chew. Unquestionably, more advanced processes are more demanding on designers (**Figure 2**). More design steps, more expensive tool licenses, and greater risk of internal iterations or silicon re-spins all add to potential costs. Even large companies kill some designs when they run out of budget before tapeout. So, both design



KEEPING MEMORY OFF THE CRITICAL PATH ON PROCESSOR PIPELINES

By Vidya Rajagopalan, MIPS Technologies

Level 1-cache-memory access is typically a critical timing path in high-performance microprocessor designs. This situation is true for processors using custom-circuit techniques, and it is an even bigger challenge for synthesizable designs. A synthesizable processor must not only meet its frequency target using SRAMs from a variety of memory vendors, but also scale well across process generations.

To achieve frequency targets, high-performance processors employ a variety of design techniques, the first and most straightforward of which is to budget enough pipeline stages for cache access. Depending on frequency targets, you can design custom processors with custom-cache subsystems such that the memory access completes in one cycle.

High-performance synthesizable processors using off-the-shelf SRAMs must, however, allow more than one cycle for memory access. The MIPS32 24K core family, for example, uses this technique, in which the instruction- and data-cache accesses each span two stages of the eight-stage pipeline. Tag- and data-RAM access takes place in the first stage, and the tag-compare and data-RAM access complete in the second. Because associative caches have become almost de facto standards, data-RAM-way selection takes place during the second stage, based on the tag comparison. As frequencies push higher, this technique falls short, because the second cycle is under pressure to do a lot of work. As a result, in the next generation of high-performance synthesizable processors, cache access completes over three cycles. The MIPS32 74K core uses this technique, which allocates three pipeline stages for cache access. It uses the first stage for tag-RAM access, the second stage for tag comparison, and the final stage for data-RAM-way selection. This technique provides a significant amount of flexibility in the timing for the data-RAM access, which the core can access in either the first or the second stage.

The three-cycle memory access also enables the use of a technique that modern EDA tools make possible. This technique involves using skew to solve the data-RAM-access bottleneck. The data RAM is larger and slower than the tag RAM. Because the critical timing path is, however, usually through tag RAM and then tag comparison, the data RAM has more time to complete its access. In the three-cycle access, data-RAM access can effectively straddle the first and second cycles, allocating more than one cycle for the array access. EDA tools can automatically determine the amount of skew necessary on the clock that drives the data RAM. Alternatively, you can manually specify the skew. The ability to use skew to move the clock edge makes it possible to scale effectively across vendor memories and process generations. These techniques represent some of the factors that allow the 74K core to achieve frequencies greater than 1 GHz in a standard 65-nm process, using generic standard cells and off-the-shelf SRAMs.

AUTHOR'S BIOGRAPHY

Vidya Rajagopalan is director of engineering at MIPS Technologies.

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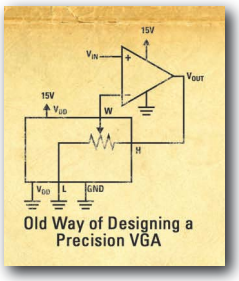

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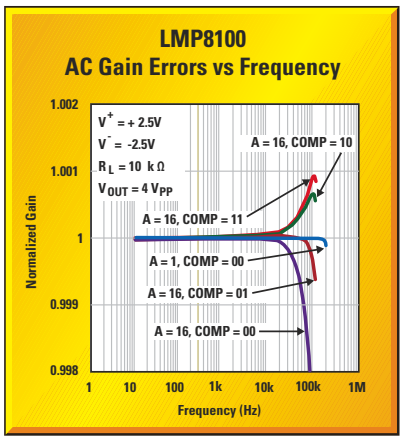

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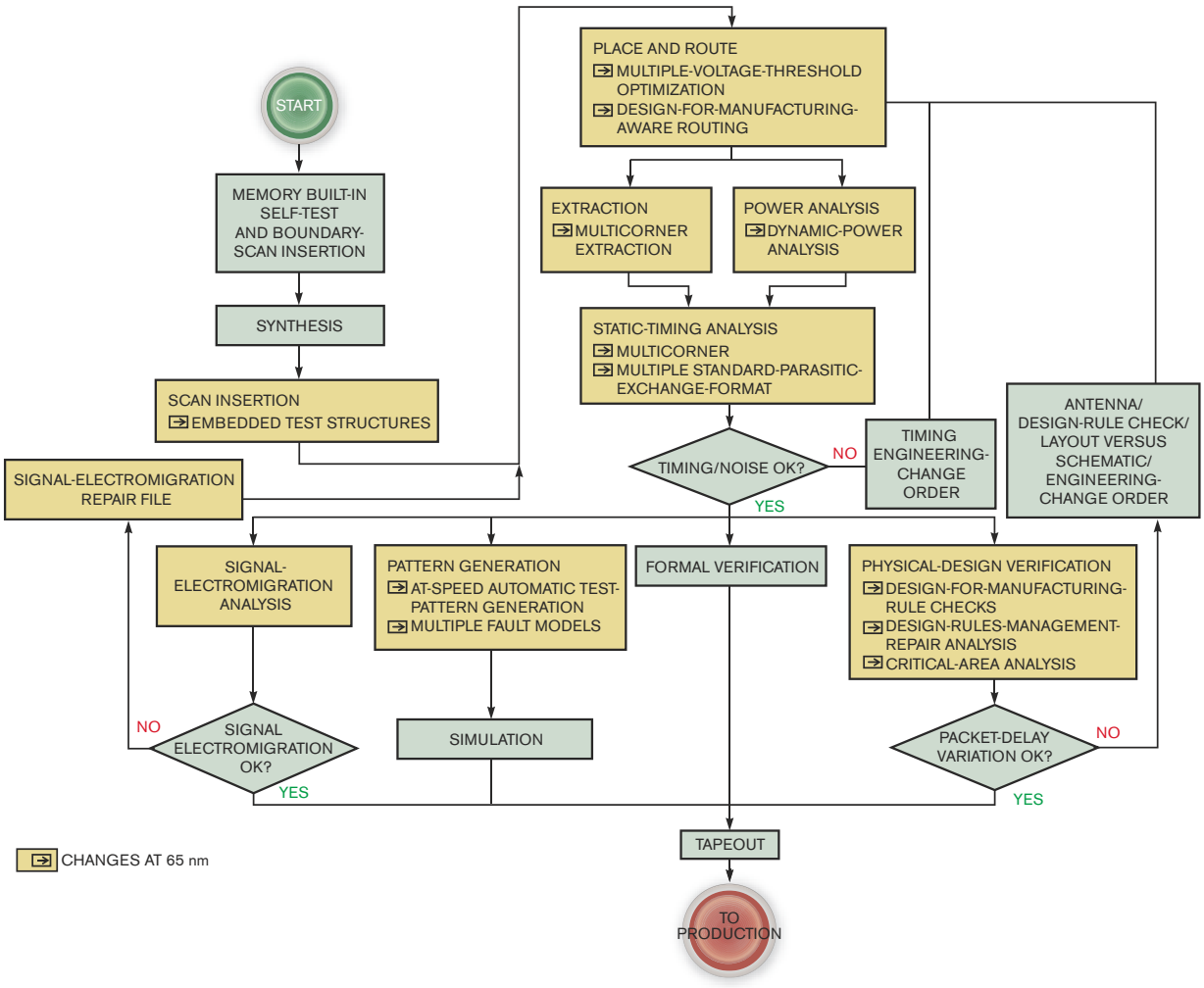

Figure 2 Moving from a 90-nm process to 65 nm adds a number of design steps (courtesy Open-Silicon).

partners and foundries try to ensure that design managers understand what they are getting into. "We train teams to do design at 65 nm," says TSMC's Paulsen. "We also recommend design partners, such as eSilicon, and we walk people through a tapeout sequence."

"We have seen design managers change their minds on their process decision at this point," Rousseau adds.

IP DILEMMAS

IP looms as the second major decision in process selection. A design team must determine what third-party IP it will need and in what processes that IP is available. "Once you've gone through the IP requirements for your design, you've pretty well made your process decision," declares Fujitsu's Stanley. There is good reason for this strong statement.

"I don't believe there is any such thing as nonsilicon-proven IP," states AMI Semiconductor's Klosterboer. "If it's not running in the process variant you intend to use, it's just a data sheet. If the IP hasn't at least been characterized from a shuttle run, the chances of a metal spin are better than 50%."

Not surprisingly, IP vendors see this situation somewhat differently. "It's true that each IP core has its own characteristics in each combination of process node, voltage, and libraries," says Gideon Intrater, vice president of solutions architecture at MIPS. But synthesizable digital IP, such as a processor core, differs from a hard analog-IP block, such as the ones ChipIdea makes. In that case, most people insist on at least test chips. The same situation was once true of critical synthesizable blocks. The variations from interactions between constraints, synthesis switches, test insertion, libraries, and design rules put too much uncertainty into the design flow for most managers. They wanted to see a CPU core in a shuttle run, in their variant, with their parameters.

But Intrater says that some IP vendors are learning to go beyond this scenario. "We are learning to make processor microarchitecture very robust at the register-transfer level," he says (see **sidebar** "Keeping memory off the critical path on processor pipelines"). This approach permits customers to hit their requirements with synthesis over a wide range of process and library choices. MIPS has synthesized its 4000 core, for instance, in processes of 65 to 250 nm. "There still are some issues," says Intrater. "For instance, core cells are starting to get faster than memory cells. In highly pipelined machines like ours, we have occasionally had to redesign SRAM cells in an advanced process so that the memory could

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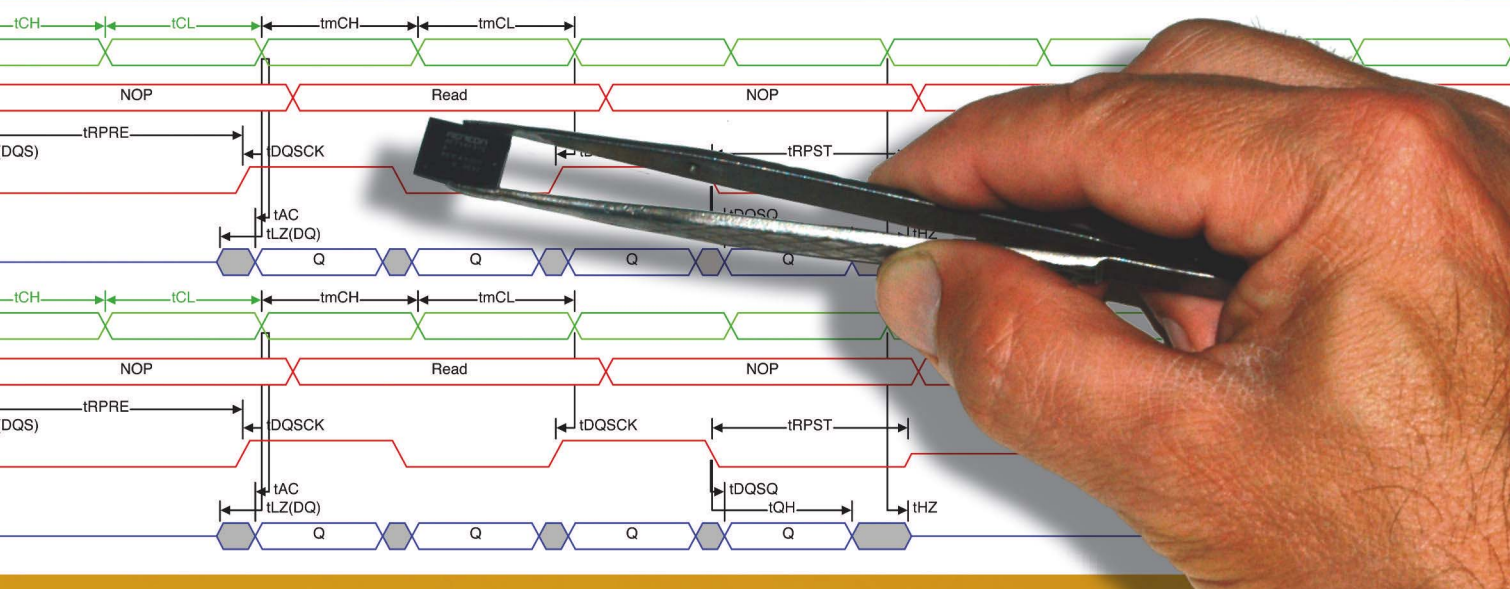

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keep up with the synthesized CPU core. Another question for the future is that it appears that, in the most advanced processes, flip-flop cells are becoming slower relative to the other cells. This [situation] could become an issue."

PERFORMANCE AND POWER

It might seem strange that I have yet to mention performance and power as decision criteria. These are increasingly design, rather than process, issues. "If you are starting a fresh design, performance is more a matter of architecture than of raw gate speed," says Paul Little, senior engineering manager at Fujitsu. "If the architecture is constrained by a previous design, then circuit speed can become a design requirement." Power is an even more complex issue. Starting at the 90-nm node, designers had to consider leakage power because it had become sufficiently larger than switching power. By the 65-nm node, you must understand the chip's application before you can begin power optimization. For example, an MP3 player that shuts off when it's not fully active differs greatly from a cell phone that is almost always in one or another standby mode.

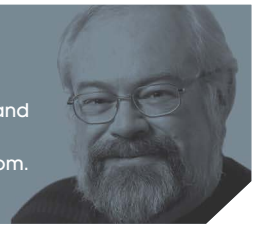
In the advanced processes, design techniques, rather than intrinsic energy efficiency, make the difference in power consumption. "We see people come in the door with a power budget in mind," says Fujitsu's Stanley. "They start out with the process characteristics, choose the grid count of their libraries based on power/performance trade-offs, and then they start adding more and more aggressive power-management techniques as necessary to meet the budget."

"Power has become a big issue for everything, not just for mobile devices," says Samsung's Hunter. "It gets much more analysis now, and it influences people's choice of process variants and libraries. For instance, we see customers coming in planning to use the general variant of the process and switching to the low-power variant when they see that, with the right techniques and libraries, they can meet their performance goals that way at lower total power."

This scenario may require designers to use different grid counts in different blocks of the design, along with voltage islands and adaptive voltage-frequency scaling. And these approaches, in turn, may influence which third-party-IP blocks are compatible with the design. You also face the risk that the details of the voltage changes will hopelessly bog down the design verification. Managing the islands could also prove too difficult for the synthesis tools. Such considerations might lead designers to go for an older process with inherently lower leakage.

None of the major variables in process selection is complex in itself. But finding even a local optimum on this complex, sometimes-discontinuous, multidimensional surface is no easy matter, even with the best estimation tools and the best, most impartial advice. The only real advantage a design manager has in the battle is that all the design partners want to succeed.**EDN**

You can reach Executive Editor Ron Wilson at 1-408-345-4427 and ronald.wilson@reedbusiness.com.



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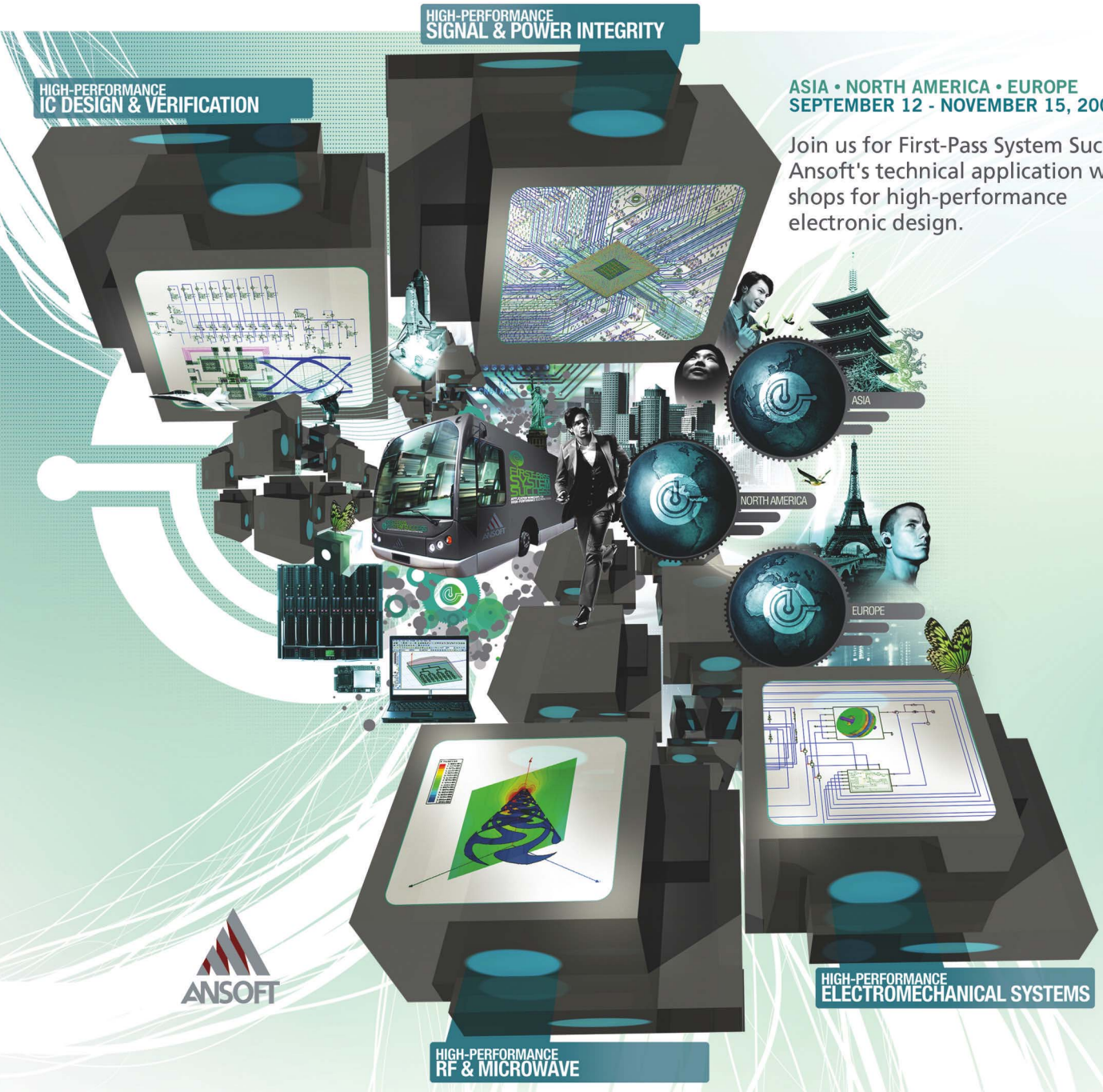

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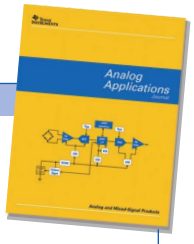
BRIEF

Get Low-Noise, Low-Ripple, High-PSRR Power with a Linear Regulator

By Jeff Falin, *Senior Applications Engineer*



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Introduction

Audio circuitry, PLLs, RF transceivers, and DACs are just a few examples of devices that can be sensitive to noise and therefore may not operate properly when powered from a switching power supply. Linear regulators are ideal for powering these circuits. This abbreviated article explores design factors required to achieve a high power-supply rejection ratio (PSRR) over a wide bandwidth with very low noise and quiescent current.

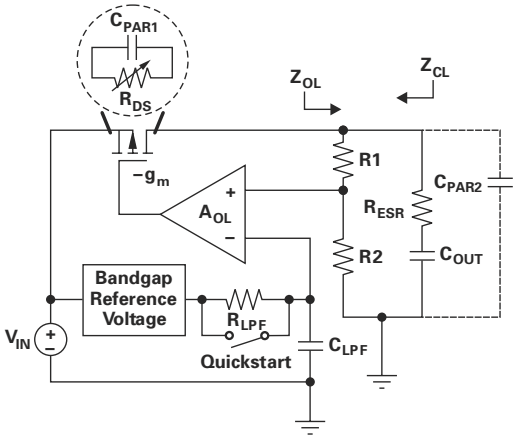

Figure 1. Simplified block diagram of a linear regulator

Figure 1 shows a simplified block diagram of a linear regulator using a p-channel MOSFET (pFET) as a pass element. A_{OL} is the open-loop gain of the error amplifier, and g_m is the pass-element transconductance. The error amplifier controls the voltage at the gate of the pass element so that the current through the FET keeps the output voltage regulated relative to the internal reference voltage. Assuming that the low-pass filter (LPF) formed by R_{LPF} and C_{LPF} eliminates nearly all internal-reference noise, the output voltage should be ripple- and noise-free for frequencies within the bandwidth of the regulator's control loop.

What is the PSRR?

The PSRR is a measure of a circuit's PSR expressed as a ratio of output noise to noise at the power-supply input. It provides a measure of how well a circuit rejects ripple at various frequencies injected from its input power supply. In the case of linear regulators, PSRR is a measure of the regulated output-voltage ripple compared to the input-voltage ripple over a wide frequency range and is expressed in decibels (dB). If the pass element in Figure 1 is treated as a variable resistance, R_{DS}, and the error amplifier and bandgap reference are assumed to have been designed to minimize pass-through of the input-voltage ripple, then the PSR is simply a voltage divider, expressed as

$$PSR = \frac{Z_{OL} \,||\, Z_{CL}}{Z_{OL} \,||\, Z_{CL} + R_{DS}}.$$

In this equation, Z_{OL} is the output impedance at the regulator's output, ignoring the effect of the regulator's feedback loop:

$$Z_{OL} = (Z_{COUT} + R_{ESR}) \,||\, (R1 + R2) \,||\, C_{PAR2},$$

where Z_{COUT} and R_{ESR} are the output capacitor's impedance and equivalent series resistance (ESR), respectively, and C_{PAR2} is the parasitic capacitance of the output components and PCB. Z_{CL} is the impedance looking back into the output of the regulator, including the effect of the regulator's feedback loop:

$$Z_{CL} = \frac{Z_{OL} \,||\, R_{DS} \,||\, C_{PAR1}}{g_m \times A_{OL} \times f \times \beta},$$

where C_{PAR1} is the passive-element parasitic capacitance, f is the ripple frequency, and β is the feedback factor,

$$\beta = \frac{R2}{R1 + R2}.$$

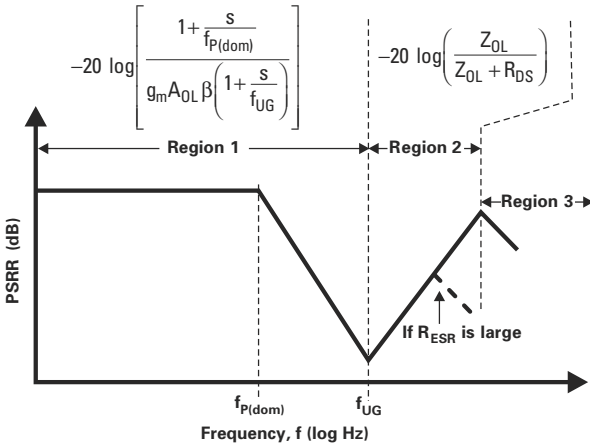

Figure 2. PSRR graph

Figure 2 shows the general shape of a PSRR curve, where $f_{P(dom)}$ is the dominant pole and f_{UG} is the unity-gain bandwidth. If the error amplifier is compensated to have a single-pole response, then the Region 1 PSR for amplifier frequencies below f_{UG} can be approximated by the equation on the left side of the graph. Designing the regulator with a high-gain, wide-bandwidth error amplifier can therefore provide high PSR over a wide range of frequencies. In Region 2, above the control-loop bandwidth, the regulator is no longer effective at providing PSR, so the PSRR reduces to a simple voltage divider as shown on the right side of the curve. As Z_{COUT} decreases relative to R_{DS}, the PSR provided by the passive components on the board increases. If C_{OUT} has high R_{ESR}, the PSR peaks sooner. In Region 3, the IC and board parasitic capacitances (C_{PAR1} and C_{PAR2}) dominate, resulting in a capacitive voltage divider, which typically causes the PSR to decrease again.

Maximizing PSR

The TPS717xx family of regulators has incorporated circuit techniques to provide high PSR over a wide frequency range. An example of the PSRR is shown in Figure 3.

With the simple model previously explained, it can be shown that the TPS717xx's dominant pole with C_{OUT} = 1 µF is at approximately 20 to 30 kHz and the unity-gain frequency is near 400 kHz. Since PSR is a function of the open-loop gain, as the gain varies so will the PSR in Regions 1 and 2 of Figure 2. Figure 3 shows the TPS717xx's PSRR varying with load current. As load current increases, R_{DS} decreases; therefore Z_{CL} decreases, since a MOSFET's output impedance is inversely proportional to its drain current. In many regulators, where $f_{P(dom)}$ varies with Z_{CL}, increasing the load current also pushes $f_{P(dom)}$ to higher frequencies, which increases the feedback-loop bandwidth. As shown in Figure 3, the net effect of increasing the load current is reduced PSRR.

The differential DC voltage between input and output also affects PSR. As $V_{IN} - V_{OUT}$ is lowered, the pFET (which provides gain) is driven out of the active (saturation) region of operation and into the triode/linear region, which causes the feedback loop to lose gain. Therefore, the PSR of the regulator decreases as V_{IN} approaches V_{OUT}. The lowest

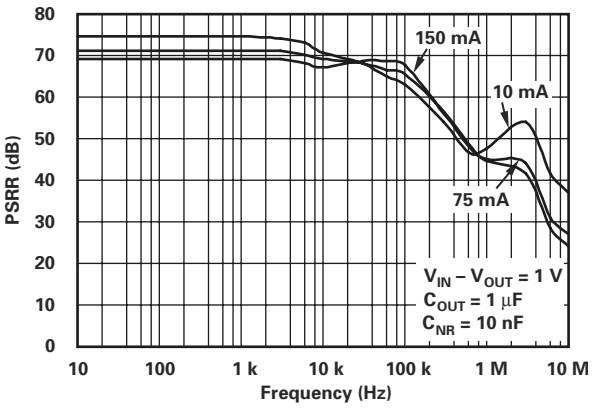

Figure 3. TPS717xx PSRR graph

PSR, approaching 0 dB, occurs when the device is in dropout ($V_{IN} \approx V_{OUT}$). In this situation, the RC filter formed by the linear regulator's pass-element R_{DS} and output capacitor determines PSR.

Low Noise

Noise is generated by the transistors and resistors in the regulator's internal circuitry as well as by the external feedback resistors. Transistors generate shot noise and flicker noise, both of which are directly proportional to current flow. Flicker noise is indirectly proportional to frequency and so is higher at low frequencies. The resistive element of MOSFETs also generates thermal noise like resistors. Thermal noise is directly proportional to temperature, the resistor's resistance value, and the current flow through the transistors. Transistors and resistors closest to the error-amplifier inputs cause the most output noise because their noise is amplified by the regulator's closed-loop gain ($A_{CL} = V_{OUT}/V_{Bandgap} = 1/\beta = 1 + R1/R2$). The noise contribution from components later in the signal path is insignificant when compared to the noise at the error-amplifier inputs. In fact, when modest-sized feedback resistors are used, most of the regulator's noise comes from the amplified bandgap reference. As shown in Figure 1, the simplest way to reduce the bandgap noise is to use a low-pass filter (LPF) consisting of an internal resistor, R_{LPF}, and an external capacitor, C_{LPF}. At startup, this filter would slow down the output-voltage rise without the aid of the "quickstart" transistor. When the quickstart transistor is used, it shorts out the R_{LPF} for a short time at startup so the regulator output can rise quickly.

Conclusion

Linear regulators like the TPS717xx are ideal for providing a low-ripple, low-noise power rail to sensitive analog circuitry. These linear regulators consume very little quiescent current when powered and even less when shut down.

Please see Reference 1 for the complete version of this article, which discusses spectral noise density, component selection, and board layout.

Reference

1. View the complete article at
http://www-s.ti.com/sc/techlit/slyt280

BY TAM DO • ALTERA CORP

Using FPGAs for HDTV design

DESIGNERS HAVE BEGUN TO APPLY DYNAMIC IMAGE-PROCESSING ALGORITHMS IN FPGAs TO CONVERT AND MAP DIGITAL-VIDEO SIGNALS ONTO DISPLAY PANELS. MULTIPLE VIDEO-PROCESSING TECHNIQUES AND BUILDING BLOCKS EXIST TO HANDLE, PROCESS, AND DISPLAY CLEAN, SMOOTH PICTURES ON FLAT-PANEL HDTVs.

Today's rapid proliferation of large-screen HDTVs (high-definition televisions) requires the use of highly complex video-processing algorithms to achieve high resolution, which in turn necessitates faster data rates to address the many artifacts that viewers would not typically notice on smaller screens. To overcome these challenges, designers are now beginning to apply dynamic image-processing algorithms in FPGAs to convert and map digital-video signals onto display panels. Designers are using many approaches for handling, processing, and displaying clean, smooth images on flat-panel HDTVs.

DESIGN CHALLENGES

The consumer market for HDTVs presents a significant challenge for product designers. To compete for the best-selling brand names, designers must consider both cost and video-performance quality. Even many ASSPs (application-specific standard products) target video-display applications; simply using only a standard IC makes it difficult to differentiate one product from another. Using available low-cost FPGAs to design a proprietary video-enhancement algorithm improves the probability of product success. FPGAs are also more effective than ASICs in shortening the design cycle. Most design groups today design an HDTV system either with a stand-alone FPGA or by coupling an FPGA with an ASSP as a coprocessor. Most FPGAs include hard-coded DSP blocks and internal memories, which form the basic elements for video and image processing.

BASIC BUILDING BLOCKS

From an architectural point of view, an HDTV usually receives a digital-TV signal from either a terrestrial or a cable/satellite set-top box (**Figure 1**). The front-end tuner demodulates the RF signal to baseband for video decoding. Typically, the decoder is either MPEG-2 or MPEG-4/H.264. HDTVs must also receive other video-signal sources, such as external-component and composite signals. The internal microcontroller multiplexes and selects all of these video-signal streams for further video processing and enhancement before the video processor maps the video pixels onto the flat-panel display.

One of the components of a video processor is a deinterlacer, which converts interlaced video to progressive video using a variety of algorithms. Television standards, such as PAL (phase-alternation line) and NTSC (National Television System Committee), commonly use interlaced video, but LCDs require progressive video, which is often more useful for subsequent image-processing functions. The basic algorithm for progressive video is the bob-or-weave algorithm. Weave deinterlacing creates an output frame by filling all of the missing lines in the current input field with lines from the previous in-

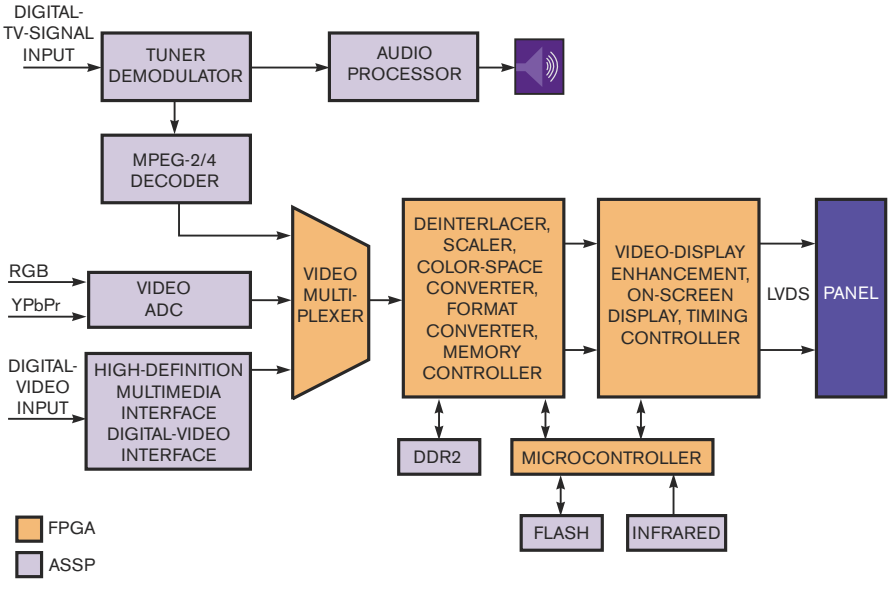

Figure 1 An HDTV usually receives a digital-TV signal from either a terrestrial or a cable/satellite set-top box.

put field. This option provides adequate results for the still parts of an image but unpleasant artifacts for the motion parts. Weave deinterlacing also requires frame-buffer storage in either on- or off-chip memory, depending on the device, to allow the weaving together of lines from different fields. For this reason, the weave deinterlacer requires a built-in triple-buffering function. Bob deinterlacing vertically scales up input fields by a factor of two. The two types of scaling for bob deinterlacing are scan-line duplication and scan-line interpolation. Scan-line duplication simply scales by twice repeating each scan line in Input Field 0 to create the output frame and discarding Input Field 1. Scan-line interpolation re-creates the lines missing from Input Field 0 by performing an unweighted mean of the lines above and below them and discarding Input Field 1. At the bottom of Field 0, only one line is available. The interpolator merely replicates this line as in scan-line duplication.

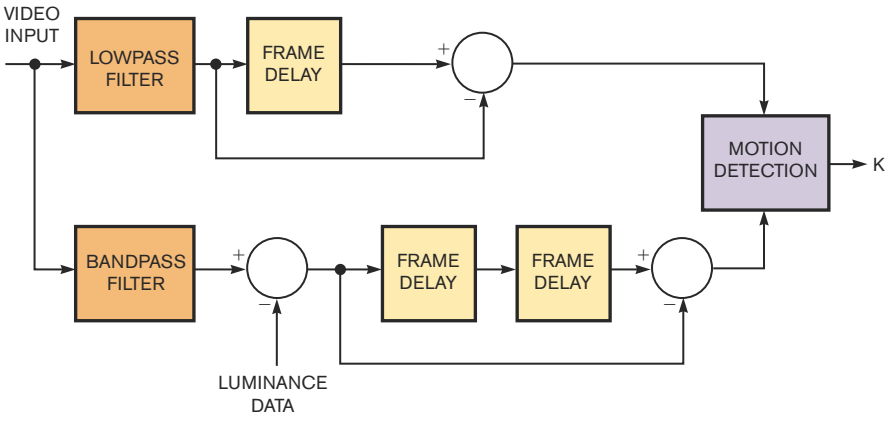

Figure 2 A basic video motion detector uses bandpass and lowpass filters.

Another enhancement algorithm, motion-adaptive deinterlacing, involves a progressive-scan-video sequence consisting of a 3-D array of data in the horizontal, vertical, and temporal dimensions (**Figure 2**). In the absence of motion, the deinterlacer identically reconstructs the interlaced sequences. In a fast-motion-video sequence, the motion detector uses the deinterlacer to separate stationary or moving areas within the same video frame. The motion-detection output uses this deinterlacer as a trigger to select either a spatial interpolation or a temporal interpolation to generate a progressive video.

Another building block in video processing is a scaler for converting video signals between arbitrary resolutions. The processor usually uses the scaler to convert low-resolution interlaced SD (standard-definition) signals to the high-resolution, noninterlaced signals that HDTV uses. A scaler's basic function is similar to that of a line doubler with extra video-signal processing and optimizing. The system designer can also use various tools and IP (intellectual property) to implement a scaler.

The human eye is less sensitive to color than to luminance. You can improve video-transmission bandwidth by storing more data affecting luminance than data affecting color. A viewer notices no perceptible loss when viewing a smaller TV panel sampling the color detail at a lower rate. Video systems achieve this feature through the use of color-difference components. They divide the signal into a Y' (luma) component and two color-difference components (chroma) in a video-camera. Larger panels require further chroma resampling to enhance the video quality of the display.

Chroma resampling deviates from color science in that the luma and the chroma components form naturally as a weighted sum of gamma-corrected R'G'B' (red/green/blue) components instead of linear-RGB components. As a result, luminance and color detail are not independent of one another; some "bleeding" of luminance and color information occurs between the luma and the chroma components. The error is greatest for highly saturated colors and can be somewhat noticeable between the magenta and the green bars of a color-bars test pattern. This approximation allows a designer to easily implement color resampling. Using this fact, video transmitted in the Y'CbCr (luminance/chroma-blue/chroma-red) color space often subsamples the color components, Cb and Cr, to save data bandwidth. The video-sampling format is Y'CbCr of 4:4:4, 4:2:2, or 4:2:0. The 4:2:2 and 4:2:0 formats are subsamples of the 4:4:4 format. How the chroma resampler performs this subsampling depends on the type of application, whether in the professional-broadcasting arena or in the consumer market. These sampling formats are parts of the MPEG-1, MPEG-2, MPEG-4, and other standards. You might wonder why standards don't use the full 4:4:4 sampling. The following video-resolution detail provides the answer: 720×486 resolution=349,920 pixels/frame; 349,920 pixels×10 bits/sample×3 samples/pixel=10,497,600 bits/frame; 10,497,600 bits/frame×29.97 frames/sec=314,613,072 bps; and 314,613,072 bps×3600 sec≃141.58 Gbytes/hour. For a

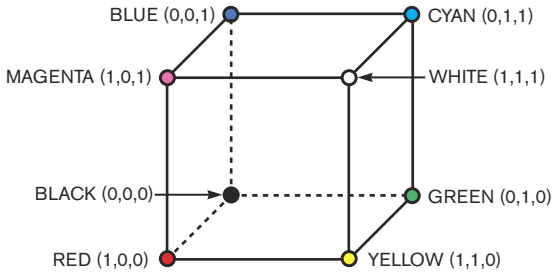

Figure 3 A color-space converter provides a flexible and efficient means of converting image data from one color space to another and provides a method for precisely specifying the display of color using a 3-D-coordinate system.

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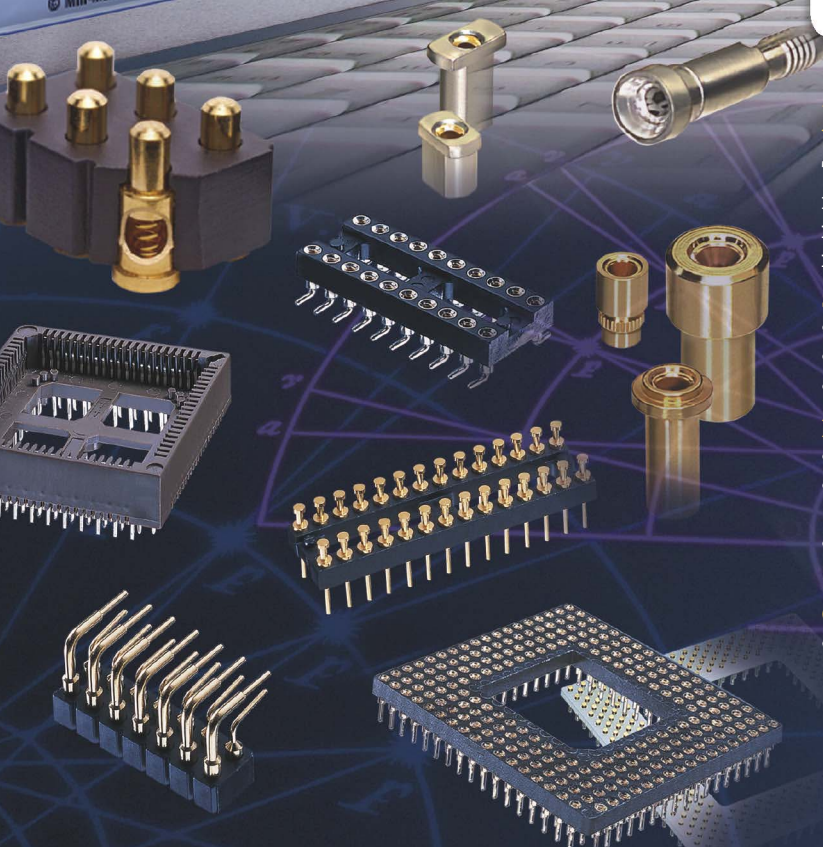

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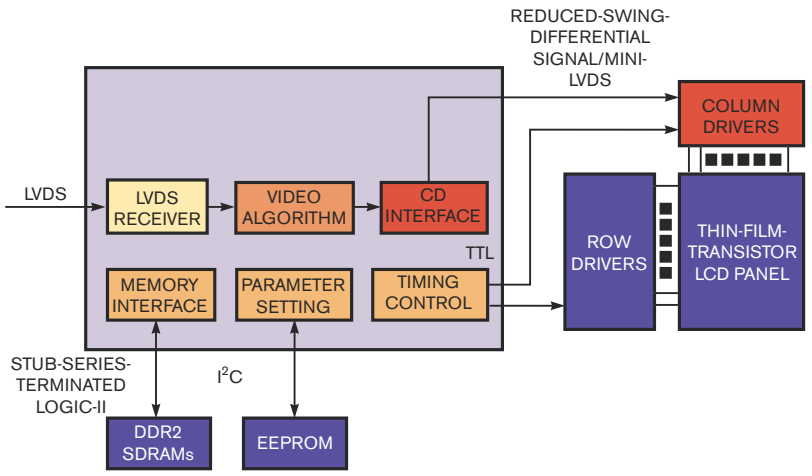

Figure 4 A timing controller is a key element of an HDTV-LCD module.

1920×1080-pixel HDTV, that figure would reach 840 Gbytes/hour. Therefore, using 4:4:4 sampling for a consumer HDTV is neither feasible nor cost-effective. A typical consumer HDTV processes a 4:2:0 video format.

A nonlinear relationship always exists between a pixel value and its displayed intensity on an HDTV monitor. This nonlinear relationship is roughly a power function: $L=V_{GAMMA}$, where L is the displayed intensity and V_{GAMMA} is the pixel value with gamma correction, a nonlinear operation that designers use to code and decode luminance values in a video-image-processing system. The gamma-correction function allows designers to modify video streams for physical properties in display devices. For example, CRTs and LCD monitors display a brightness that has a nonlinear response to the voltage of a video signal. To account for this response, designers program the gamma-correction function with a look-up table that models the nonlinear function and then use that function to transform the video data and produce the best image on the display.

FIR AND MEDIAN FILTERING

One of the most common video-enhancement blocks is the FIR (finite-impulse-response) filter. A FIR filter multiplies and sums a sequence of received-video-data impulses, creating a 2-D convolution process. A 2-D FIR filter can perform 2-D convolution using matrices of 3×3, 5×5, or 7×7 coefficients. A 2-D FIR filter's key provides sharpening, smoothing, and edge detection of a video image. By designing the proper coefficients and applying the correct matrix, you can produce a crystal-clear video output. However, the electrical system can introduce video noise into a video stream during transmission in any channel. A median filter provides a simple and effective noise-filtering process. The median value of all the pixels in a population—that is, a selected neighborhood block—determines each video pixel. The median value of a population is that value in which one-half of the population has smaller values than the median and the other half has larger values than the median value.

You can combine an OSD (on-screen display) and an alpha-blending mixer to provide a method to layer streams of video onto a display screen with text and other graphics. One of the most common applications is the EPG (electronic-programming guide) for an HDTV display. A typical valid range of alpha coefficients is [0, 1], where 1 represents full translucence and 0 represents full opaqueness. For N-bit RGBA (red/green/blue-alpha) values), the range is [0, 2N–1]. This range interprets (2N−1) as 1 and all other values as the alpha value

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divided by 2N. For example, 8-bit alpha value (255=>1), (254=>254÷256), (253=>253÷256), and so on. Implementing OSD in an FPGA is fairly straightforward. You use a local microcontroller either within or outside the FPGA to generate the graphics or text characters, and you use a video-line buffer to mix the generated text.

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A color-space converter provides a flexible and efficient means of converting image data from one color space to another and provides a method for precisely specifying the display of color using a 3-D-coordinate system (**Figure 3**). Different color spaces are appropriate for different display devices, such as R'G'B' for computer monitors or Y'CbCr for HDTV. Color-space conversion is often necessary when transferring data between devices that use different color-space models. For example, to transfer a TV image to a computer monitor, you must convert the image from the Y'CbCr color space to the R'G'B' color space. Conversely, transferring an image from a computer display to a TV may require a transformation from the R'G'B' color space to Y'CbCr. Video displays for SDTV and HDTV require different conversions, such as to or from the Y'IQ (perceived-luminance/color-luminance-information) model for NTSC systems or the Y'UV (luminance-bandwidth-chrominance) color model for PAL systems.

You achieve conversions between color spaces by providing an array of nine constant coefficients and three constant summands that relate the color spaces. Given the constant coefficients A0, A1, A2, B0, B1, B2, C0, C1, and C2 and the constant summands S0, S1, and S2, you calculate the output values on channels 0, 1, and 2 (d_{OUT0}, d_{OUT1}, and d_{OUT2}): $d_{OUT0}=(A0\times d_{IN0})+(B0\times d_{IN1})+(C0\times d_{IN2})+S0$; $d_{OUT1}=(A1\times d_{IN0})+(B1\times d_{IN1})+(C1\times d_{IN2})+S1$; and $d_{OUT2}=(A2\times d_{IN0})+(B2\times d_{IN1})+(C2\times d_{IN2})+S2$.

CONTROLLER AND INTERFACE

A timing controller is a key element of an HDTV-LCD module (**Figure 4**). It is the last building block you implement after the video processor has performed all video processing and signal enhancement and before interfacing to the display panel. The controller must correctly map all video color pixels on the display with precise timing without incurring video-quality degradation. As in the past, designers currently implement these controllers using fully customized ASIC devices or ASSPs. Neither of these types of devices provides the full scalability of an FPGA, which allows you to scale a design for a small display to a large display. FPGAs also provide a built-in LVDS (low-voltage-differential-signal)- or RSDS (reduced-swing-differential-signal)-interface format that the timing controller typically uses to directly drive the HDTV-display panel. You can program FPGA-based timing controllers to support nonstandard resolutions and different LCD-panel configurations from various LCD manufacturers.

Designers have over the last two years made significant improvements in the quality of image processing for HDTV flat-panel displays. In addition to a variety of standard available ASSPs, designers are now using low-cost FPGAs with built-in features, such as DSP blocks, memories, microcontrollers, and differential interfaces, to leverage the rapid design cycle. FPGAs can serve as standalone units or as complements to an ASSP-system design to provide superior video enhancement for the digital-TV-display market. EDN

AUTHOR'S BIOGRAPHY

Tam Do is a senior technical-marketing manager at Altera Corp, where he is responsible for defining and developing technical systems and marketing plans for the professional-broadcast and consumer-electronics arenas. Do holds a bachelor's degree in electrical engineering from University of Nevada—Reno, and his personal interests include ham radio. You can reach him at tamdo@altera.com or at his ham-radio call sign, N7EQR.

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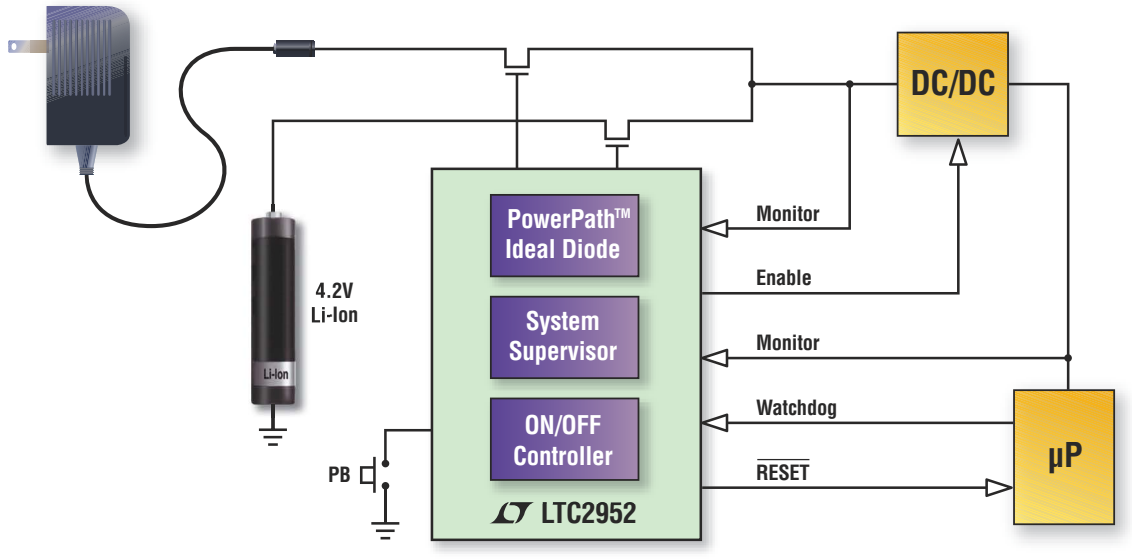

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LTC2954	2.7 to 26	6µA	Adj	Adj		Interrupt logic for menu driven applications. Active high enable output (LTC2954-1), active low enable output (LTC2954-2)	TSOT-8, DFN-8

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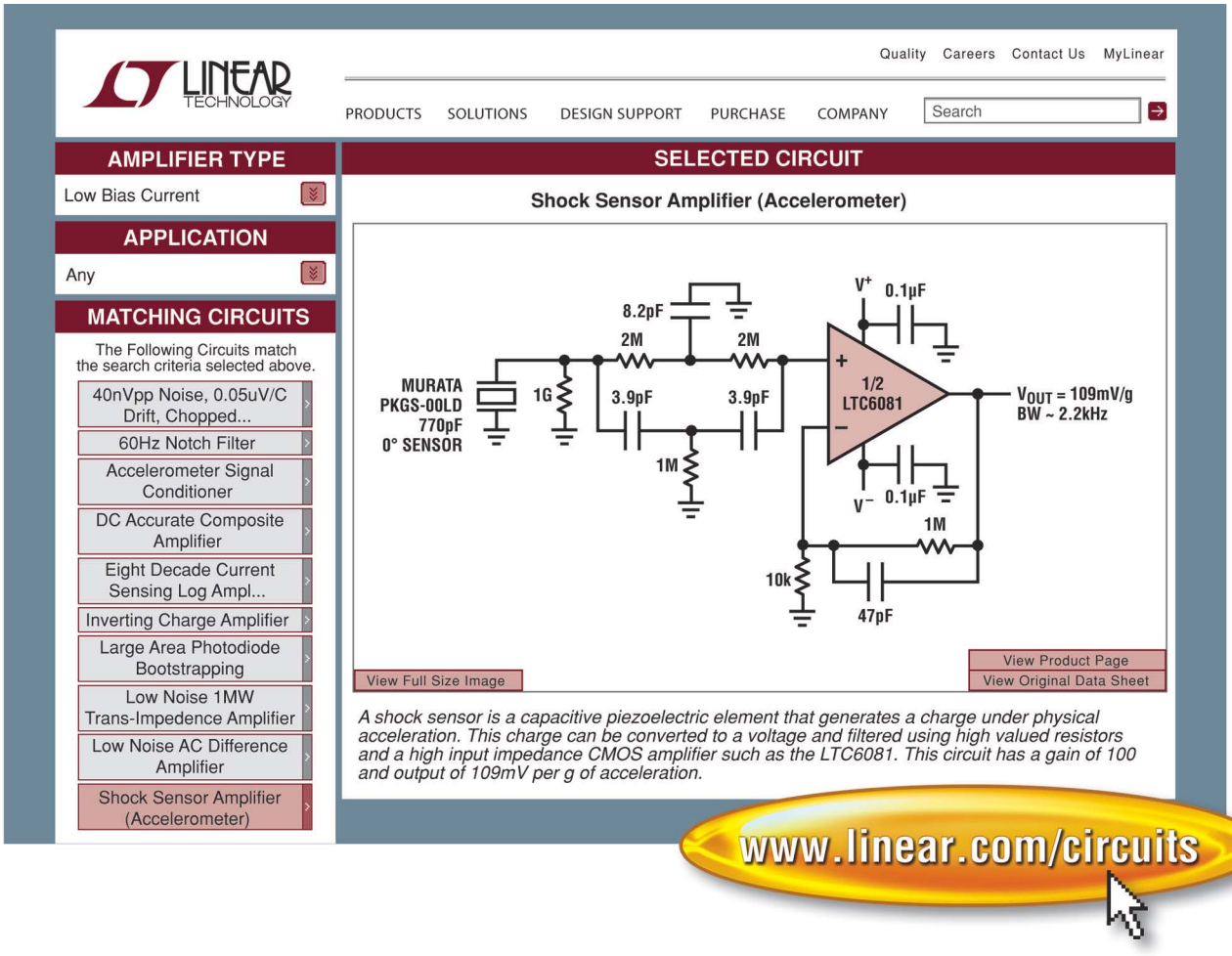

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LTC6087	1	750	14	1.2	2	General Purpose	MS-8, DFN-10
LTC6088	1	750	14	1.2	4	General Purpose	DFN-16, SSOP-16
LTC6078	0.2	25	0.75	0.072	2	TCV_{OS} = 0.7µV/°C Max.	MS-8, DFN-10
LTC6079	0.2	25	0.75	0.072	4	TCV_{OS} = 1.4µV/°C Max.	DFN-16, SSOP-16
LTC6240	0.2	175	18	2.4	1	Low Frequency Noise = 550nV_{P-P}	SOT-23-5, SO-8
LTC6241	0.2	125	18	2.2	2	Low Frequency Noise = 550nV_{P-P}	DFN-8, SO-8
LTC6242	0.2	150	18	2.2	4	Low Frequency Noise = 550nV_{P-P}	DFN-16, SSOP-16
LTC6244	1	100	50	5.8	2	Low Frequency Noise = 1.5µV_{P-P}	DFN-8, MS-8

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READERS SOLVE DESIGN PROBLEMS

Flexible Hopfield neural-network ADCs quash noise

Paul J Rose, PhD, Mental Automation, Renton, WA

A Hopfield network can convert analog signals into digital format and can perform associative recalling, signal estimation, and combinatorial optimization similar to the way a human retina performs first-level signal processing. This Design Idea explores the Hopfield-neural-network paradigm for ADCs.

Simple converters comprise one-layer neurons that accept analog inputs and generate digital-bit outputs; such neurons make up one form of adaptive- and distributive-processing networks. These neurons comprise voltage comparators driving either analog inverters or followers and fully connected feedback resistors from the analog outputs of the inverters or followers to the comparators (**figures 1** and **2**). Reference and analog-input voltages drive the neural networks, and digital outputs come from the comparators in the networks. Hopfield networks have learning capabilities; the circuit in this Design Idea can apply different adaptive-learning rules by using alternative comparator-inverter/comparator-follower schemes, conductance-node-layout schemes—reciprocals of the feedback resistances—between the input comparators, and bit-order readouts.

As the analog-input voltage increases, the circuit can produce either monotonically increasing (from a comparator-inverter scheme) or decreasing (from a comparator-follower scheme) bit-word outputs. Decreasing outputs are the complements of increasing outputs and suggest subtractive-bit operations. Further, you can shape the digital responses of the converters to analog-input voltages in varying degrees using different conductance-node layouts as part of rule adaptation. For further flexibility, reversing bit order for digital readouts allows for reflection of circuit responses about analog-input/digital-output characteristics.

You can simply state a few symbols and their meanings to construct the two converters. For energy functions, the resistive network conductances—synapse weightings (S) in the form of reciprocal resistances (R)—have the designations $S_{IJ}=1/R_{IJ}$, where I is the Ith input comparator, J is the Jth feedback path to the Ith comparator, and I does not equal J—that is, there is no self-feedback path of the comparator to itself. The conductance between the input terminal of the Ith comparator and the reference voltage, V_R, has the designation $S_{IR}=1/R_{IR}$. The conductance between the input terminal of the Ith comparator and the analog-input-signal voltage, V_S, has the designation $S_{IS}=1/R_{IS}$.

For graphical curve fittings, Y is the normalized output-bit variable, and X is the normalized input analog voltage from a nonzero average value (less than one) to one. A, B, and C are curve-fitting constants in the curve equation $Y=1-A\times(1-X)^C$ and the complementary-curve equation $Y=A\times(1-X)^C$, where A is a coefficient, B is the lower limit for X and is less than one, and C is a power con-

TABLE 1 INPUT VOLTAGE VERSUS OUTPUT WORD

Input analog voltage (V)			Output binary word	
Raw range	Normalized range	Average normalized range	Raw	Normalized
0 to 0.189	0 to 0.2855	0.1427	0	0
0.189 to 0.265	0.2855 to 0.4003	0.3429	1000	0.5333
0.265 to 0.378	0.4003 to 0.571	0.4856	1100	0.8
0.378 to 0.662	0.571 to 1	0.7855	1110	0.933
More than 0.662	1	1	1111	1

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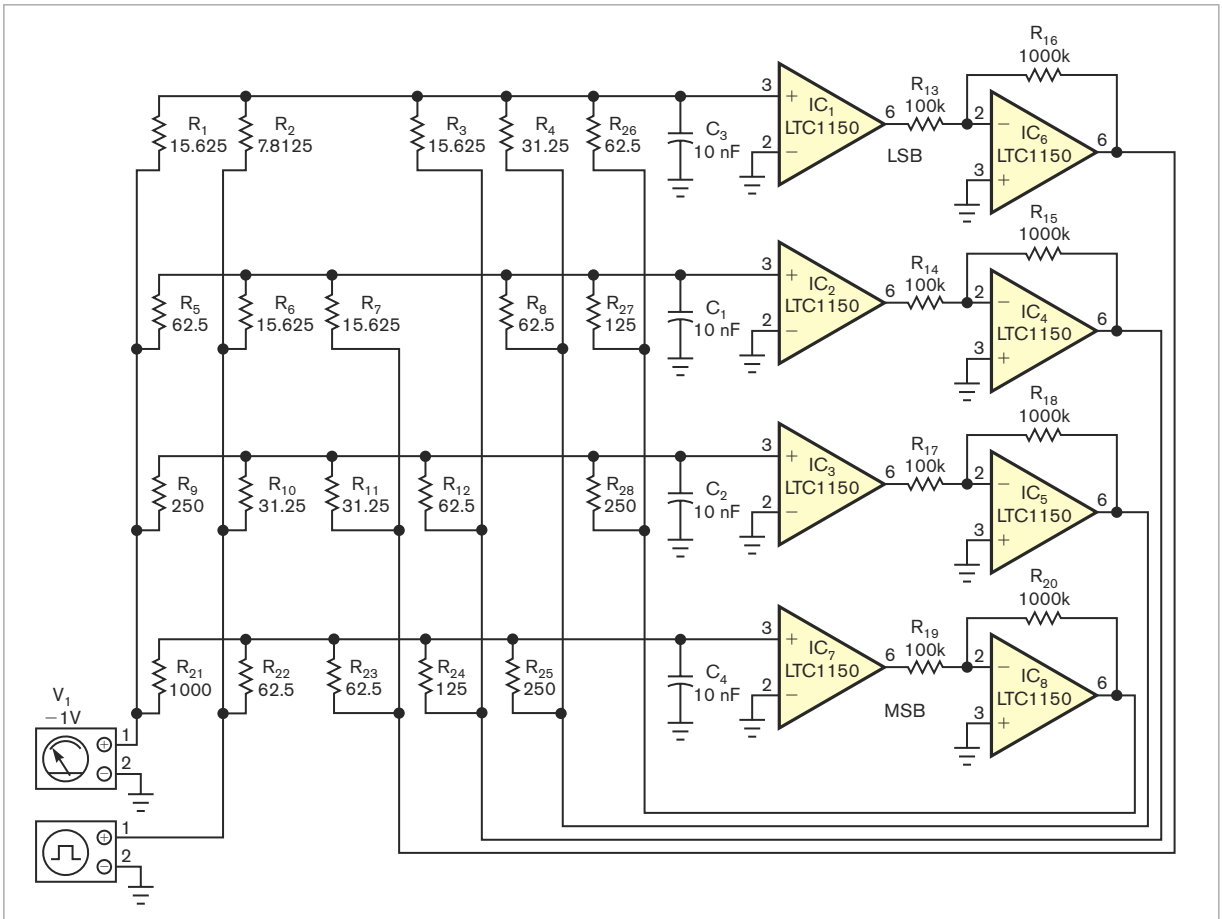


Figure 1 This Hopfield neural ADC provides a robust output in the presence of noise.

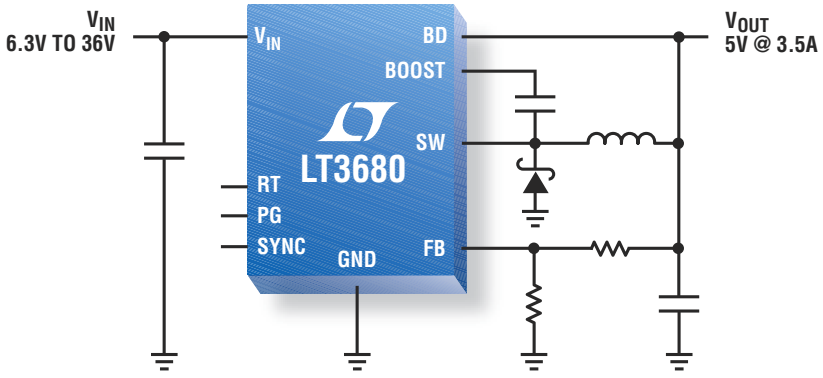
stant. For bit-pattern readout reversals, you can have the curve equation $Y=A\times(X-B)^C$ and the complementary-curve equation $Y=1-A\times(X-B)^C$.

Figure 1 shows a 4-bit neural ADC employing voltage inverters that comparators feed. The comparators connect with their positive terminals joined to input nodes and with their negative terminals grounded. The bases of this network are inverse factors of one-half—that is, reciprocal factors of two—input-node conductances $S_{IJ}=-1\times2^{(2-I-J)}$, where the −1 factor comes from negative feedback through the related resistor; $S_{IR}=2^{(1-2\times I)}$; and $S_{IS}=2^{(1-I)}$. To determine node resistances, choose a maximum node resistance of 1000Ω corresponding to a minimum conductance of 0.0078125, and a minimum node resistance of 7.8125Ω corresponding to a maximum conductance of one. Calculate all other resistances from the ratios between the extremes of conductances. Using these values, you can construct **Table 1**. The **table** lists bits ranging from the most significant bit to the least significant. The **table** shows that the digitization process is inaccurate in that it is not linear with input voltage and with many intermediate bit words missing. But the process is precise because it is repeatable over sizable input-voltage ranges. From the **table**, you can derive the following curve-fitting **equation**: $Y=1-1.6243\times(1-X)^{3.1508}$. When X is over the normalized range of 0.1427 to 1, A=1.6243, B=0.1427, and C=3.1508. The Y **equation** is essentially cubic, and it quantitatively shows the highly nonlinear nature of the digitization process. You can obtain a "flipped" mirror—that is, not a true mirror, or pseudoscopic—version of the curve of the straight line on a normalized graph by reversing the bit-order readout from the circuit so that the resulting curve equation would be: $Y=1.6243\times(X-0.1427)^{3.1508}$.

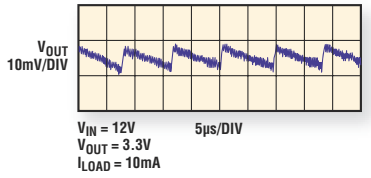
Without analog-input-voltage transformation, such as the use of look-up tables or logarithmic amplifiers to process the input voltage, or digital corrective logic, digital responses from simple Hopfield neural converters are nonlinear and crude. However, these responses are still possibly useful for such applications as associative memory and pattern classification because of robustness in output precision.

Indeed, because of output digital stability, the Hopfield neural converter can allow for unwanted analog-input-signal noisiness or variations. This scenario is in strong contrast to conventional interface circuits between analog-transmission media and digital-

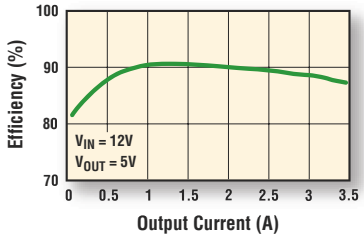
36V Buck Converters



Burst Mode® Output Ripple



Efficiency



2.4MHz, 3.5A I_{OUT}, 75µA I_Q, 10mV_{P-P} Ripple, 3mm x 3mm DFN

Linear's growing family of 36V input-capable buck converters has the performance and features demanded by automotive, industrial and medical applications. These devices have programmable and synchronizable high frequency operation to keep externals small and high efficiency conversion to minimize thermal issues. Many devices feature micropower operation, suitable for always-on applications. With very low output ripple from no-load to full load, these converters reduce noise and provide best-in-class output currents in compact packages.

Selected 36V+ Buck Converters

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LT®3470	4V to 40V	0.2	Hysteretic Mode	26µA	2 x 3 DFN-8, ThinSOT™
LT3502/A	3V to 40V	0.5	1.1MHz/2.2MHz	1.5mA	2 x 2 DFN-8
LT3505	3.6V to 36V, 40V Max.	1.4	300kHz to 3MHz	2mA	2 x 3 DFN-8, MSOP-8E
LT3681	3.6V to 34V, 36V Max.	2.0	300kHz to 2.8MHz	50µA	3 x 4 DFN-14
LT3684	3.6V to 34V, 36V Max.	2.0	300kHz to 2.8MHz	0.85mA	3 x 3 DFN-10, MSOP-10E
LT3481	3.6V to 34V, 36V Max.	2.0	300kHz to 2.8MHz	50µA	3 x 3 DFN-10, MSOP-10E
LT3685	3.6V to 38V, 60V Max.	2.0	200kHz to 2.4MHz	0.85mA	3 x 3 DFN-10, MSOP-10E
LT3480	3.6V to 38V, 60V Max.	2.0	200kHz to 2.4MHz	70µA	3 x 3 DFN-10, MSOP-10E
LT3680	3.6V to 36V	3.5	200kHz to 2.4MHz	75µA	3 x 3 DFN-10, MSOP-10E
LT3508	3.7V to 36V, 40V Max.	1.4 x 2	250kHz to 2.5MHz	4.6mA	4 x 4 QFN-24, TSSOP-16E

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computing machines. This Design Idea shows that flexible circuit adaptability can exist in producing various forms of stable digital outputs from neural ADCs depending on a designer's needs for neural-network-signal processing. This adaptability can be in the forms of various input-node-conductance layouts; comparator/inverter and comparator/follower combinations; and the selected order of bit-readout patterns from the comparators.EDN

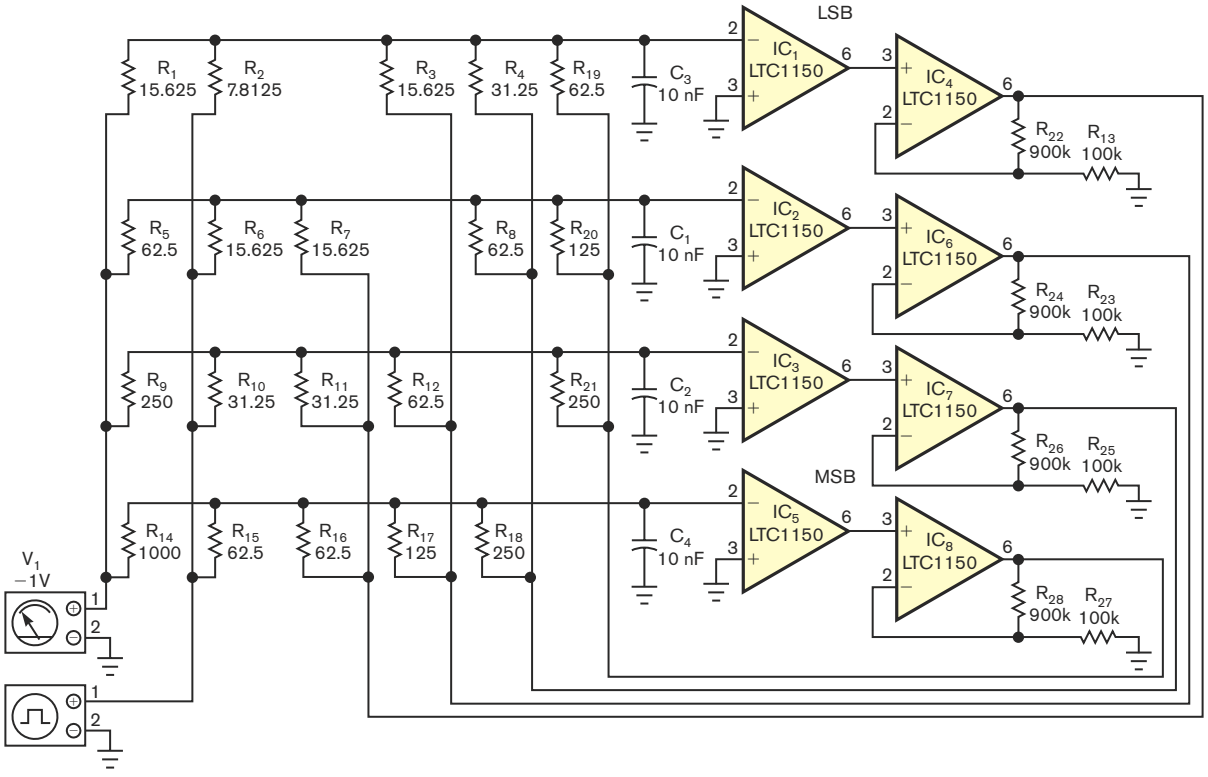

Figure 2 This version of the Hopfield neural ADC features inverted bit outputs.

8-bit microcontroller implements digital lowpass filter

Abel Raynus, Armatron International, Malden, MA

Filtering occurs frequently in the analog world. Unfortunately, in the digital world, engineers apply it mainly to the DSPs (digital-signal processors) and not to the small 8-bit microcontrollers that designers commonly use. This situation occurs because the math for the filter design is more complicated than most engineers are willing to deal with. Moreover, digital filtering requires calculations on integers instead of on floating-point numbers. This scenario causes two problems. First, the rounding-off error from the limited number of bits can degrade the filter response or even make it unstable. Second, you must handle the fractional values with integer math.

Several ways exist to solve these issues. For example, you can use operations with 16-, 32-, and 64-bit numbers, or you can scale for better accuracy. These and other methods usually require more memory, and, as a result, the program often does not fit into a small microcontroller. A literature search shows that published digital-filter firmware is written in C. Programs in C need more memory than those written in assembler. This situation often makes them unacceptable for small microcontrollers with limited memory resources.

Listing 1, available at the Web version of this Design Idea at www.edn.com/080124di1, shows a simple engineering method to design single-pole, lowpass-digital-filter firmware for 8-bit microcontrollers. The low-end Freescale (www.freescale.com) MC68HC908QT2 is the target of the assembler program, but you can apply this Design Idea to any type of microcontroller because it uses only standard assembler instructions.

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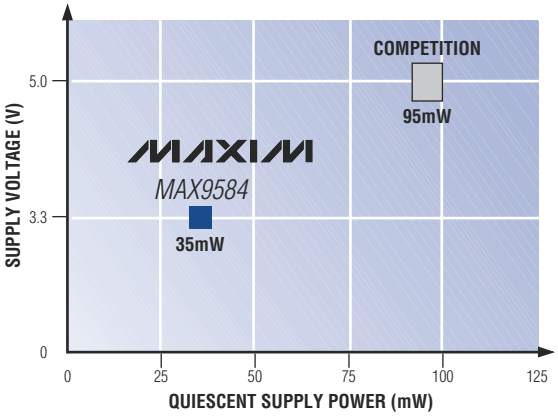

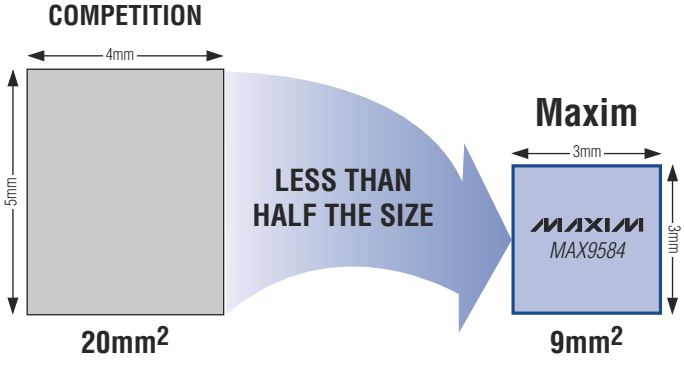

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Leaving aside the sophisticated design methods based on Z transformation with its extensive math, this idea uses another approach based on a recursive equation. You calculate each output-signal sample as the sum of the input signal and the previous output signal with corresponding coefficients. A recursive equation defines a single-pole lowpass filter as: $Y[n]=X[n]\times a0+Y[n-1]\times b1$, where X[n] and Y[n] are input and output values of sample [n], Y[n-1] is an output value of the previous sample [n−1], and a0 and b1 are weight coefficients that decrement δ controls. The coefficients have the value of $0<\delta<1$, $a0=1-\delta$, and $b1=\delta$. Physically, δ is the amount of decay between adjacent output samples when the input signal drops from a high level to a low level. You can directly specify the value of δ or find it from the desired time constant of the filter, d, which is the number of samples it takes the output to rise to 63.2% of the steady-state level for a lowpass filter. A fixed relationship exists between d and δ: $\delta=e^{-1/d}$, where e is the base of natural logarithms. The preceding **equations** yield $Y[n]=Y[n-1]+(1-\delta)\times(X[n]-Y[n-1])$.

NUMERICALLY PERFORMING THE FILTERING FUNCTION PROVIDES THE BENEFIT OF CONSISTENCY BECAUSE COMPONENT TOLERANCES, TEMPERATURE DRIFT, AND AGING DO NOT AFFECT THE FILTER'S ALGORITHM.

Instead of multiplying a decimal-point number, $1-\delta$, it is more convenient for assembler programming to divide by the reciprocal integer, $F=1/(1-\delta)$: $Y[n]=Y[n-1]+(X[n]-Y[n-1])/F$. Thus, you can determine the digital filter's parameters using the following steps:

1. Choose the parameter F. For assembler, it is convenient to perform division as right shifts. For right shifts, the value of F should be 2S, where S is the number of shifts. Let F equal 8, which you reach after three right shifts.

2. Calculate the decrement: $\delta=1-1/F=1-1/8=0.875$.

3. Calculate the time constant as $d=-1/\ln\delta=-1/\ln 0.875=7.49$ samples.

The **equation** $Y[n]=Y[n-1]+(X[n]-Y[n-1])/F$ determines the design of the microcontroller's algorithm for the filter. The algorithm needs three registers: input for X[n], output for Y[n], and an increment register to keep the $(X[n]-Y[n-1])/F$ term. The size of these registers depends on the inputs. In this application, the signals from the built-in 8-bit ADC range from 00 to $FF and must go through the lowpass filter. So, the input and the output registers are 1 byte in size. To increase the accuracy of division, add half the divisor to the dividend. This action increases the increment register to 2 bytes.

Numerically performing the filtering function provides the benefit of consistency because component tolerances, temperature drift, and aging do not affect the filter's algorithm. The implementation of the digital filter in the microcontroller gives the additional benefit of flexibility to adjust the filter's parameters, because this flexibility depends only on the firmware. EDN

Automotive switching regulators get input-transient-voltage protection

Kevin Daugherty, National Semiconductor, Novi, MI

Engineers often face difficult trade-offs when voltage regulators can encounter high-voltage transients that are well above normal input-supply operating ranges. This situation is common in automotive applications in which high-voltage transients from an alternator load dump can produce transients of 36 to 75V for durations as long as 400 msec. Designers must choose between a regulator that can withstand such maximum input voltage or use an input-protection scheme. The simple circuit in this Design Idea provides a highly cost-effective method for clamping an input voltage from a battery input with transients as high as 50V to take advantage of a 20V, 3-MHz regulator. With this circuit, your design can achieve a small total footprint with relatively low cost because of the 3-MHz operation along with lower voltage components than might otherwise be necessary to withstand 50V.

Input-protection components consist of Q_1, R_1, D_1, C_5, and one-half of D_2 (**Figure 1**). At start-up, N-channel MOSFET Q_1's source is at ground potential and turns on when R_1 applies the battery voltage to the gate. Once the input voltage is above the minimum of 2.74V on IC_1, the LM2734Z regulator starts switching, which charges the bootstrap circuit comprising D_3, D_4, and C_B. This bootstrap voltage of approximately $V_{OUT}-V_{FD}$ (forward-voltage drop) of D_3 then transfers to the gate source of Q_1. Capacitor C_5 then maintains gate drive during the bootstrap diode's off times.

Under normal operating conditions, for example, the battery voltage is 8 to 18V, D_1 does not limit conduction of Q_1, and the gate voltage tracks approximately 2.5V above the input-supply voltage for a low voltage drop from the battery voltage to the input voltage of the LM2734Z. However, when the input voltage increases above the threshold that D_1 sets, the input voltage to the LM2734Z regulates to the zener voltage (V_Z) of D_1 minus the threshold voltage of Q_1, or approximately $20-2V=18V$, well below the 24V absolute maximum of the LM2734Z. Selecting Q_1 requires careful consideration of maximum input voltage, gate-to-source-voltage threshold, and power dissipation under both steady-state and thermal-transient conditions.

Q_1, the SI1470DN N-channel MOSFET, provides 50V protection

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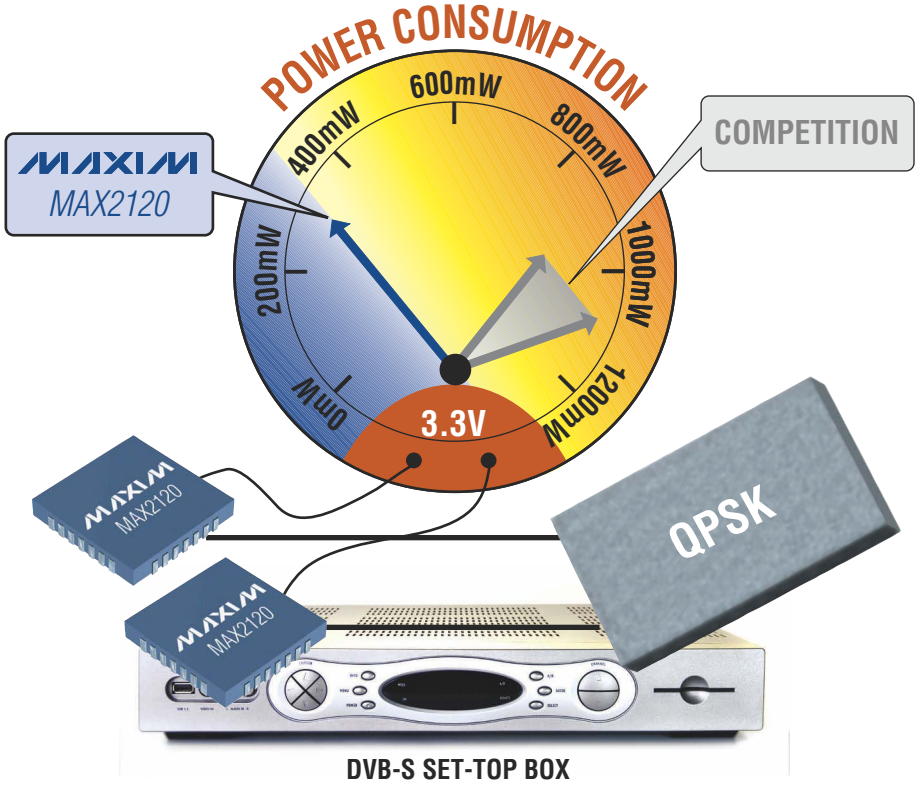

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with a drain-to-source voltage (V_{DS}) of 30V+20V (zener diode D_1 voltage), has an on-resistance of 95 mΩ at a gate-to-source voltage of 2.5V, and comes in a thermally efficient SC70-6 package. For some applications, the regulator's output voltage may be insufficient to fully turn on the selected protection MOSFET, so you can increase the bootstrap voltage with a separate zener reference, as the LM2734Z's data sheet shows (**Reference 1**).EDN

REFERENCE

1 "LM2734Z Thin SOT23 1A Load Step-Down DC-DC Regulator," National Semiconductor, www.national.com/pf/LM/LM2734Z.html.

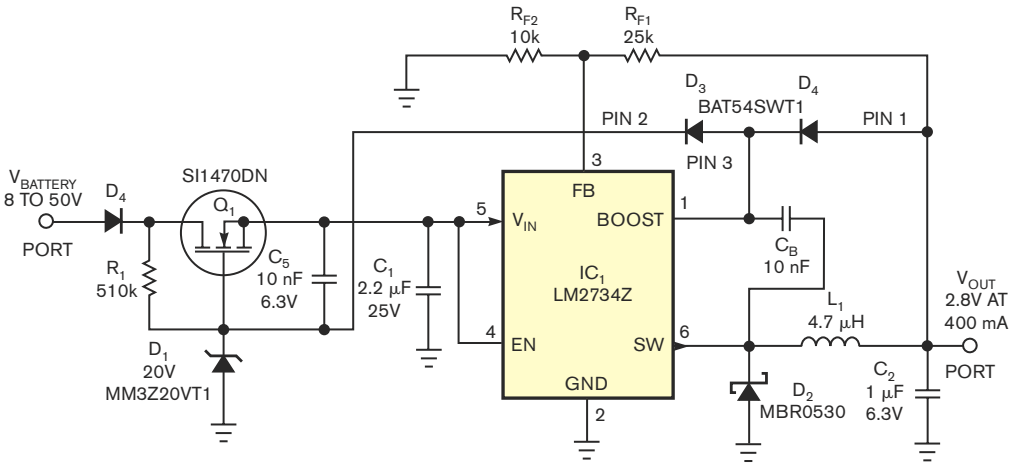

Figure 1 The N-channel MOSFET and zener diode protect the switching regulator against transient voltages as high as 50V in automotive applications.

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DESIGN NOTES

A Positive-to-Negative Voltage Converter Can Be Used for Stable Outputs Even with a Widely Varying Input – Design Note 433

Victor Khasiev

An obvious application of a positive-to-negative converter is generating a negative voltage output from a positive input. However, a not-so-obvious use is to produce a stable output voltage in an application that has a widely varying input. For example, a converter in a battery-powered device, which has an inherently variable input voltage, can produce a stable output voltage even if input voltage falls below the absolute value of the output voltage. However, an obvious drawback is reverse polarity, which can be easily overcome in this application. The supplied circuitry can use the negative output as the system ground and the negative battery terminal as the "positive" voltage source.

This topology is particularly useful when the input varies above or below the output. In such cases, a traditional step-down regulator would not be able to regulate once the battery voltage drops below the output, thus shortening the useful battery run time. Buck-boost solutions and other topologies such as a SEPIC solve this problem, but they tend to be more complicated and expensive. The positive-to-negative converter topology presented here combines the simplicity of a step-down converter and the regulation range of a buck-boost topology.

A new generation of Linear Technology high voltage synchronous step-down converters, such as the LT®3845, make it possible to implement positive-to-negative conversions for a variety of applications.

Basic Operation

Figure 1 shows a simplified block diagram of a positive-to-negative converter. Figure 2 shows an equivalent circuit, which helps in understanding the basic operation of the circuit in Figure 1. When transistor Q is on (Figure 2a), diode D is reverse biased and the current in inductor L increases. When Q is off (Figure 2b), inductor L changes polarity, diode D becomes forward biased, and current flows from inductor L to the load and capacitor C. The voltage across capacitor C and the load is negative, relative to system ground. Figure 3 shows a timing diagram.

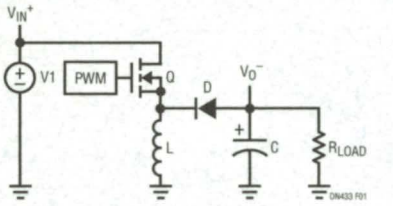
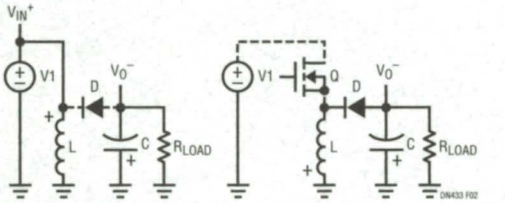


Figure 1. Simplifed Block Diagram of Positive-to-Negative Converter



(2a) Transistor Q is On (2b) Transistor Q is Off

Figure 2. Equivalent Circuits Show the Operation of the Positive-to-Negative Converter

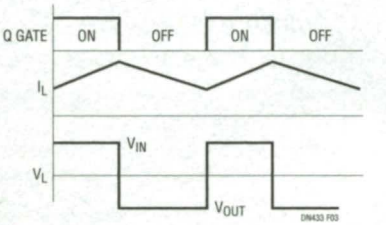


Figure 3. Converter Timing Diagram

The duty cycle range can be found from following expression:

$$D = \frac{|V_O|}{V_{IN} + |V_O|}$$

$$D_{MAX} = \frac{|V_O|}{V_{IN(MIN)} + |V_O|}$$

$$D_{MIN} = \frac{|V_O|}{V_{IN(MAX)} + |V_O|}$$

Component Stress in a Positive-to-Negative Topology

V_{MAX} is the maximum voltage across transistor Q and diode D (Figure 2), where:

$$V_{MAX} = V_{IN(MAX)} + |V_O|$$

The maximum current, I_{MAX}, through transistor Q, inductor L and diode D can be derived based on the following equations, assuming continuous conduction mode:

$$I_L = \frac{I_O}{1-D_{MAX}},\ dI = \frac{V_{IN(MIN)} \bullet t \bullet D_{MAX}}{L},\ I_{MAX} = I_L + \frac{dI}{2}$$

where t is a switching period.

Circuit Description

Figure 4 shows a 9V to 15V input to –12V at 3A output converter. The high voltage LT3845 is used for several reasons, including the ability of its SW pin to withstand 65V, its integrated high side driver and differential current sense. The LT3845 can also provide synchronous rectification, which allows the use of efficient MOSFETs over less efficient switching diodes.

The entire converter power path contains the LT3845 high voltage PWM controller, MOSFETs Q1 and Q2, inductor L1, diode D1 and output filter capacitors C_{OUT1}–C_{OUT3}. Diode D2 is a bootstrap diode and diode D3 provides bias voltage for internal MOSFET drivers.

Conclusion

Very often electrical engineers have to design a negative voltage source supplied from a positive voltage rail. The positive-to-negative converter discussed in the article can be a good alternative to a flyback or a SEPIC approach.

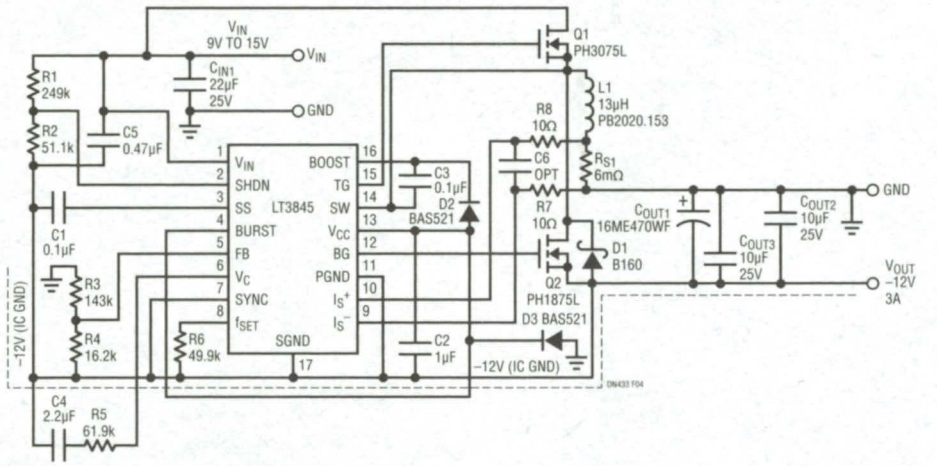


Figure 4. Conversion of 9V-15V into –12V at 3A Based on the LT3845 High Voltage PWM Controller

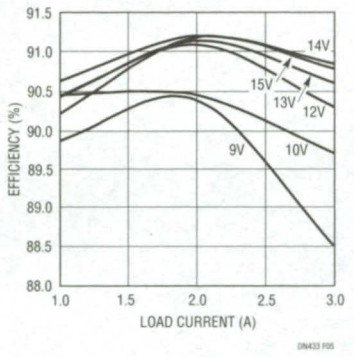


Figure 5. Efficiency for the Figure 4 Circuit with Varying Input Voltage to a Fixed –12V Output

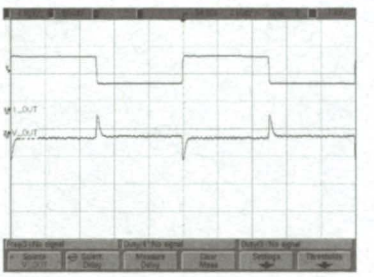


Figure 6. Transient Response to an Output Load Step of 1A to 2A

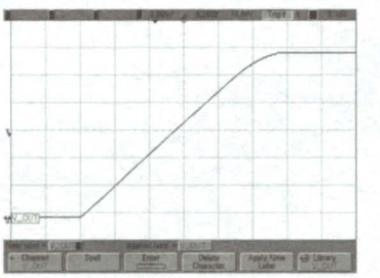


Figure 7. Start-Up Waveform for the Circuit in Figure 4 with V_{IN} = 14V, V_{OUT} = –12V, I_{OUT} = 2A

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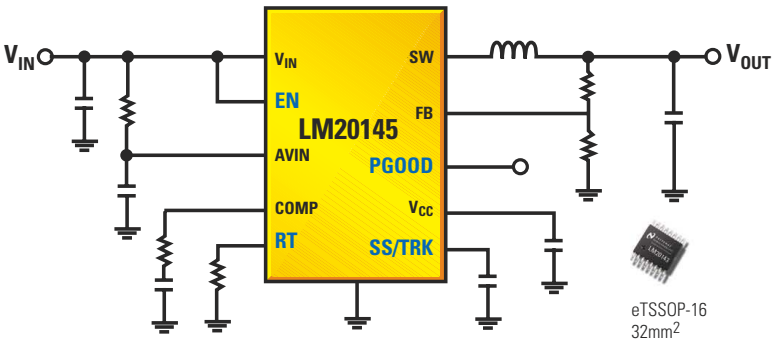
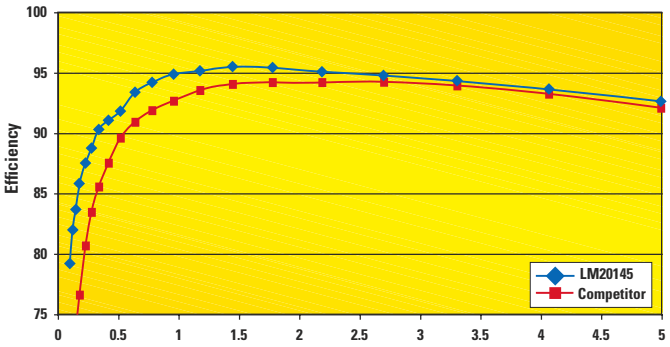


Efficiency vs Output Current (V_{IN} = 5.0V, V_{OUT} = 3.3V, fSW = 500 kHz)



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LM20133	2.95 to 5.5	3	✔			Sync
LM20143	2.95 to 5.5	3		✔		500 kHz - 1.5 MHz
LM20124	2.95 to 5.5	4				1 MHz
LM20134	2.95 to 5.5	4	✔			Sync
LM20144	2.95 to 5.5	4		✔		500 kHz - 1.5 MHz
LM20154	2.95 to 5.5	4			✔	1 MHz
LM20125	2.95 to 5.5	5				500 kHz
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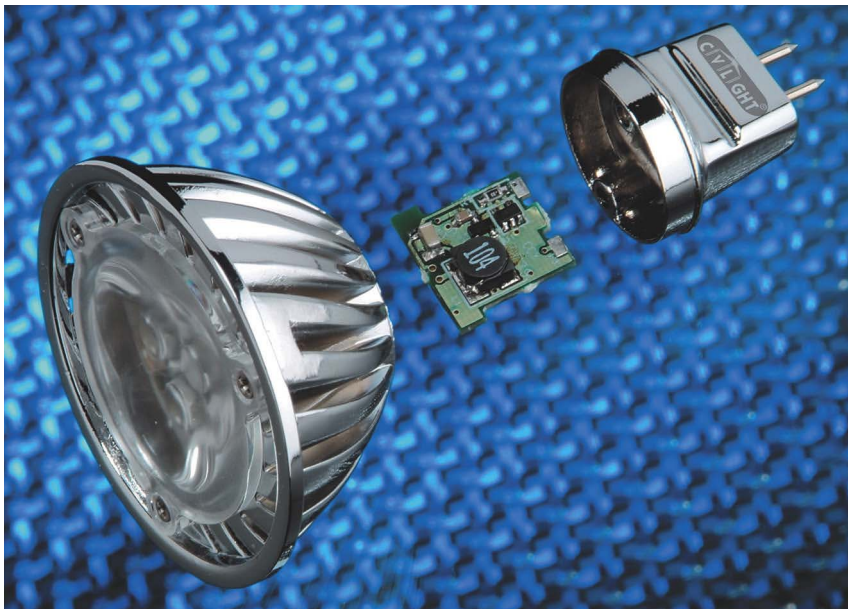


MR16 chip set and reference design reduce component count by 50%

Aiming at MR16-compatible LED lamps, the MR16 dedicated chip set and reference design have 50% fewer components than similar products, as well as decreasing PCB (printed-circuit-board) size and weight in lamp necks. Suiting use in associated-power-rectification, LED-current-control, and protection functions, the devices enhance lighting-class LEDs' reduced total cost of ownership, compared with that of halogen-reflector lamps. The MR16 costs 90 cents (1000).
Zetex Semiconductors, www.zetex.com

1W LEDs provide two and three luminous-flux options

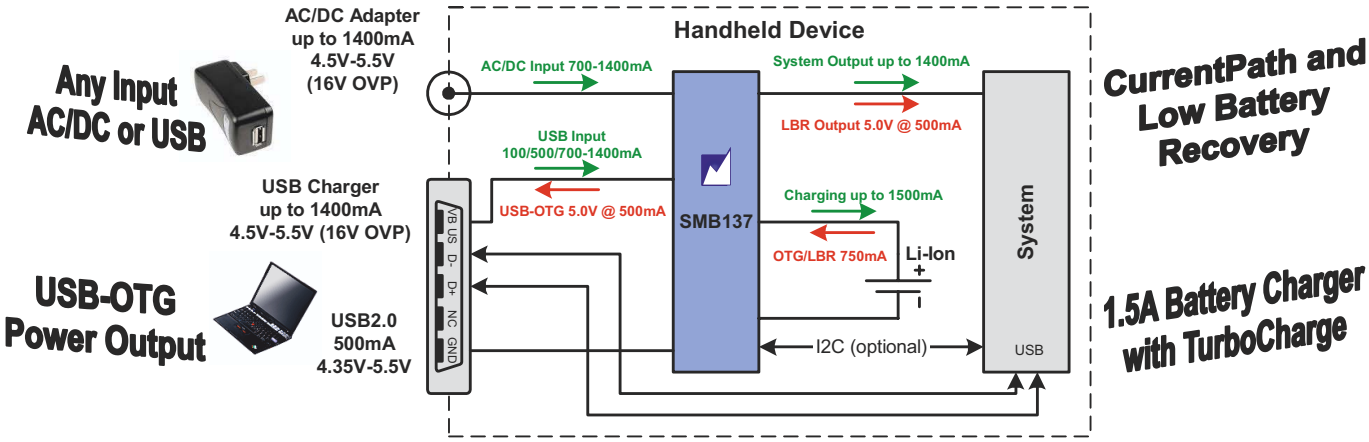
The high-brightness, 1W Little Star LEDs come in yellow, amber, warm white, and white. Amber and yellow LEDs provide two luminous-flux options; the white VLMW711x and the warm-white VLMW71x versions have three luminous-flux options. Features include an 18 and 20K/W thermal resistance, a 7150- to 22,400-mcd high-luminous intensity, and a 21,000- to 70,000-mlm luminous flux. Each device offers a 60° half-intensity angle and a 120° viewing angle, and the devices are IR-reflow-solder-process-compatible. Available in an SMD power package with a 6×6×1.5-mm footprint, the Little Star amber and yellow LEDs cost 70 cents, and the warm-white and white LEDs range from $1 to $1.50.
Vishay Intertechnology, www.vishay.com

Three-channel LED drivers provide independent-channel PWM dimming

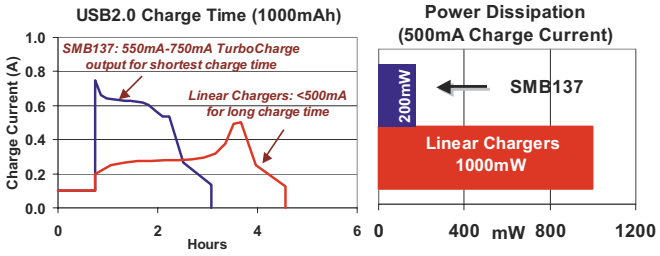
The high-voltage, high-brightness MAX16824 and MAX16825 three-channel LED drivers allow independent-channel PWM (pulse-width-modulation) dimming and LED cur-

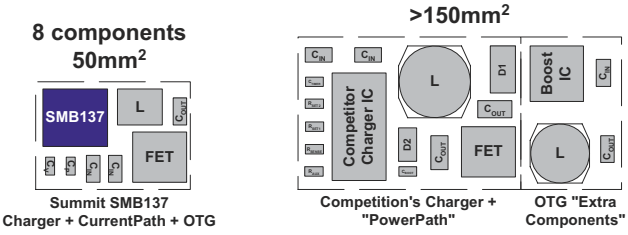
Solve Input Power and Battery Charging Challenges with One Flexible Chip

SMB137 Supports Any Input, Output or Battery Configuration. Charging and Power Management -Without Extra Components



Reduce Charging Time by 50% Cut Power Dissipation by 75% Shrink Solution Size by 66%





*Patent(s) pending

Features

- CurrentPath™ for "instant-on" from dead battery
  - *Dual input USB or AC/DC with auto-select*
  - *Dual output – System Output and Charger*
- TurboCharge™* - 750mA from USB, 1.5A from AC/DC
- Low-Battery Recovery™ Mode* (LBR™) to "boot" from dead battery and enumerate USB port
- USB On-the-Go (OTG) Power (+5V @ 500mA)
- I²C Programmable Input/Output/Charging Parameters
- Built-in OV/OC/Thermal/Timer Safety
  - *IEEE1725 Compliant*
- 3mm x 3mm CSP Packaging

Applications

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- Handheld GPS Terminals
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rent adjustment. Features include a 6.5 to 28V input-voltage range and three 36V-rated, open-drain, constant-current sink outputs delivering as much as 150 mA to three strings of high-brightness LEDs. The ICs allow independent LED-current setting for each channel. The MAX16824 provides three PWM dimming inputs, allows independent control of the brightness of each string of LEDs, and allows the switching on or off of each string. The MAX16825 features a 3-bit transparent latch; a 3-bit shift register; and a 3-Mbps, four-wire serial interface. The serial interface allows the control of output channels through an external microcontroller and allows cascading of MAX16825 drivers for combined operation. The device provides a 5V regulated output with a 4-mA output-current capability and thermal shutdown in the event of overheating. Available in a 4×4-mm TSSOP-16 package with an exposed pad, the MAX16824 and MAX16825 LED drivers cost 91 cents each (1000).

Maxim Integrated Products, www.maxim-ic.com

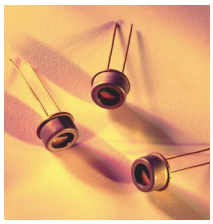
Quad-mode fractional-charge pump requires no additional capacitors

The CAT3604V quad-mode fractional-charge pump drives as many as four LEDs. Quad-mode technology provides inductor-based LED-driver efficiency levels and claims to eliminate high-profile inductors and EMI (electromagnetic interference). In addition to the three operating modes typical for charge-pump LED drivers and corresponding to the ratio of V_{OUT} to V_{IN} (1×, 1.5×, and 2×), the device adds a fourth, 1.33×. Requiring no additional capacitor, the 1.33× fractional-operating mode reduces the input-switching currents at the battery, reducing supply noise. Additional features include high average efficiency; a PWM (pulse-width-modulation) dimming interface; and channel diagnostics, including automatic detection for short- and open-LED-channel conditions. The CAT3604V costs 48 cents (10,000).

Catalyst Semiconductor, www.catsemi.com

980-nm laser diodes feature quantum-well-intermixing technology

Using quantum-well-intermixing technology, the 980-nm, high-power HPD Series 6100 single-emitter laser diodes provide as much as 200 mW of power. The process increases



the quantum-well bandgap of a semiconductor laser in a controlled manner, allowing the creation of active and passive sections in the same laser cavity. The process creates the passive nonabsorbing mirrors in the facet regions of the cavities and avoids catastrophic optical-mirror damage that typical laser devices frequently encounter. The devices have wavelengths of 980±5 and 980±10 nm, and additional wavelengths are available on request. Available in 5.6- and 9-mm and C-mount packages, the HPD Series 6100 costs $200.

Intense Ltd, www.intenseco.com

Constant-current LED driver targets automotive lighting

Operating over typical automotive battery and temperature ranges, the automotive-grade, high-brightness A6260 constant-current LED-driver IC provides a 6 to 40V input-voltage range. Users can adjust linear constant-current output to deliver 350 mA in a typical application. The LED driver suits automotive-interior lighting, such as map lights and dome lights, and exterior lighting,

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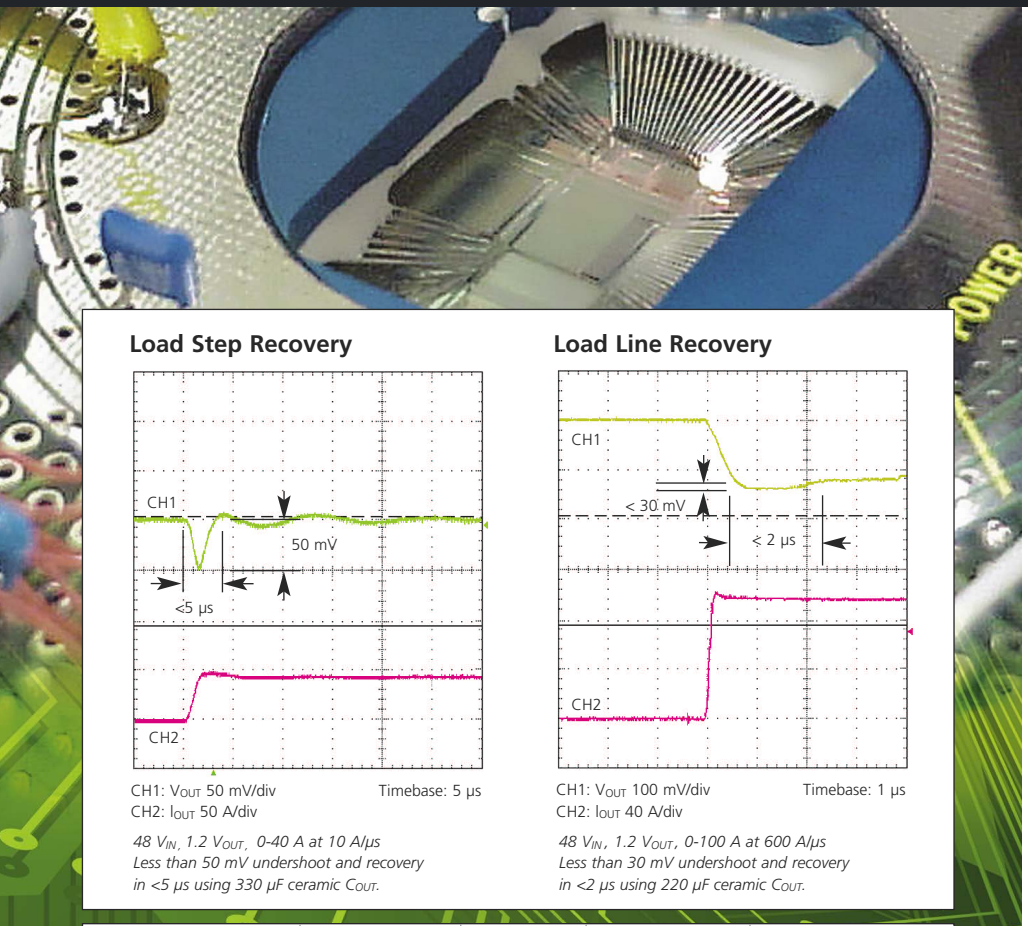
V•I Chip power components provide fast response and maintain power integrity



Load Step Recovery

CH1: V_{OUT} 50 mV/div
CH2: I_{OUT} 50 A/div
Timebase: 5 µs

48 V_{IN}, 1.2 V_{OUT}, 0-40 A at 10 A/µs
Less than 50 mV undershoot and recovery
in <5 µs using 330 µF ceramic C_{OUT}.

Load Line Recovery

CH1: V_{OUT} 100 mV/div
CH2: I_{OUT} 40 A/div
Timebase: 1 µs

48 V_{IN}, 1.2 V_{OUT}, 0-100 A at 600 A/µs
Less than 30 mV undershoot and recovery
in <2 µs using 220 µF ceramic C_{OUT}.

Product Listing

PRM Model No.	V_{IN} Nominal (V)	V_{OUT} Range (V)	Output Power (W)	Efficiency @ Full Load (%)
P024F048T12AL	24	26 - 55	120	95.0
P048F048T24AL	48	36 - 75	240	96.0
P045F048T32AL	48	38 - 55	320	97.0

VTM Model No.	V_{OUT} Nominal (V)	V_{OUT} Range (V)	Output Current (A)	Efficiency @ 50% Load (%)
V048F015T100	1.5	0.81 - 1.72	100	91.0
V048F020T080	2.0	1.08 - 2.29	80	94.2
V048F120T25	12.0	6.50 - 13.75	25	95.1

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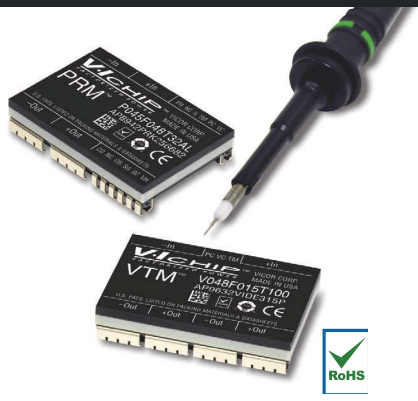

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including rear indicator lights, brake lights, and rear combination lighting. A temperature-monitor chip causes the output current to reduce in a foldback fashion, and the foldback is adjustable by choosing an appropriate resistor. Available in an SOIC-8 package, the A6260 LED driver costs 85 cents (1000).

Allegro Microsystems, www.allegromicro.com

COMPUTERS AND PERIPHERALS

Two-port eSATA device runs at 3 Gbps

Suiting use with the PCIe (PCI Express) interface, the 1225SA dual-port eSATA (external-serial-advanced-technology-attachment) device provides 3 Gbps. The device uses Host-RAID (redundant array of inexpensive disks), an integrated RAID technology configurable as two individual ports with no RAID JBOD (just a bunch of disks), with RAID 0 striping, or with RAID 1 mirroring. The device also features eSATA hot-swap compatibility. The two-port 1225SA PCIe RAID controller costs $75.

Adaptec, www.adaptec.com

PCI adapter allows four Compact Flash cards in multiple configurations

Aiding in the creation of a low-cost, large-scale-capacity SSD (solid-state drive), the AD4CFPRJ PCI adapter adds as many as four Compact Flash cards to any system with RAID (redundant-array-of-inexpensive-disks) support. Built-in firmware allows the configuration of four Compact Flash cards as a single large volume; of four individual drives; or for redundancy supporting RAID 0 striped, RAID 1 mirrored, and RAID 10 mirrored striped. Supporting UDMA (ultradirect-memory access), DMA (direct-memory access), and PIO (programmed-I/O) hard-drive modes, the adapter's operating-system support includes DOS, Windows 98/ME, NT 4.0, 2000, XP, Vista, and Linux kernel 2.4+. The AD4CFPRJ PCI adapter costs $49.95.

Addonics Technologies, www.addonics.com

Port-to-DVI/HDMI level shifter comes in lead-free "green" packages

The PI3VDP411LS dual-mode-display-port-to-DVI/HDMI (digital-visual-interface/high-definition-multimedia-interface) level shifter converts four differential, low-swing ac-coupled inputs to HDMI Revision 1.3-compliant outputs. Key features include 3.3 to 5V DDC (direct-digital control) and an HPD (high-priority-data) level shifter, 2.5-Gbps HDMI level shifting per lane required for 36-bit deep color, and integrated 50Ω termination resistors for ac-coupled differential inputs. Available in lead-free and environmentally friendly packages, the PI3VDP411LS costs $1.30, and the PI3VDP411LSZDE costs $1.50 (10,000).

Pericom Semiconductor, www.pericom.com

DAC provides 128-dB SNR

The high-performance WM8741 stereo DAC delivers 128-dB SNR (signal-to-noise-ratio) monophonic and advanced digital-filter options. Features include group delay, phase and latency, and impulse-response and transition-band roll-off. The system provides a dithered digital-interpolation filter, fine-resolution volume control, digital-enable de-emphasis, a multibit sigma-

productroundup

COMPUTERS AND PERIPHERALS

delta modulator, and a switched-capacitor multibit stage with differential voltage outputs. Available in an SSOP-28 package, the WM8741 DAC costs $6.71 (10,000).

Wolfson Microelectronics, www.wolfsonmicro.com

ExpressCard adapter allows systems to run any CardBus device

The ADEXC34CB ExpressCard adapter allows users to run CardBus peripherals through the high-speed ExpressCard port. The adapter supports single-lane, 2.5-Gbps PCIe (PCI Express), compliance with the 32-bit PC Card Cardbus, and a hot-plug capability through the ExpressCard connector. The ADEXC34CB adapter features Windows 98/ME, 2000, XP, 2003, Vista, and Mac OS compatibility. The ADEXC34CB costs $69.95.

Addonics Technologies, www.addonics.com

1- and 3-Tbyte servers come in rack-mount and desktop versions

The 1-Tbyte, four-drive StorCenter Pro NAS (network-attached-storage) 200r print servers and the 3-Tbyte desktop-NAS StorCenter Pro NAS 150d server with active-directory-support devices are available in rack-mount and desktop versions. The 200r and the 150d NAS devices use a 10/100/1000-Mbps GbE (Gigabit Ethernet) port connecting to four SATA-II (serial-advanced-technology-attachment-II) drives configurable for RAID (redundant-array-of-inexpensive-disks) 0 striping, RAID 1 mirroring, or RAID 5 striping-plus-parity operation. Providing hot-swappable hard drives, the 200r and 150d servers support clients running Microsoft Windows Vista, 2000/XP Home/XP Professional, and XP Professional 64; MAC OS X 10.2.7 or higher; and Linux distributions, including Redhat9, Madrake 10, Debian 3, Gentoo, and FedoraCore3. Network-file-protocol support includes Microsoft, Linux/Unix, Apple, Internet, and FTP. The StorCenter Pro NAS 150d server costs $1699, the StorCenter Pro NAS 200r server costs $1899, and the StorCenter Pro NAS 200r server with print capability costs $2499.

Iomega Corp, www.iomega.com

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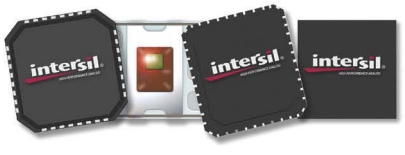

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  - Boost
  - Charge Pumps
  - System Power
- Backlight LED Drivers

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LOOKING AHEAD

TO DESIGN AUTOMATION AND TEST EUROPE 2008

The DATE (Design Automation and Test Europe) conference will run from March 10 through 14 in Munich, Germany. Although many still think of the conference as the strictly European little brother of the much larger Design Automation Conference in the United States, this event has grown to attract a unique set of technical papers and special topic sessions, making it worth consideration for North American engineers, as well. Papers give a much better view into vital European research and development and reflect markets that are better developed in Europe, such as ultra-low-power systems, mobile TV, and automotive electronics. The special topics this year—dependable embedded systems and automotive electronics—are good examples.

LOOKING BACK

TO FIELD COMMUNICATIONS BEFORE SATELLITE RADIO

A compact, air-transportable radio-communication terminal with an antenna that inflates like a balloon is in evaluation by the US Army. Designed by Collins Radio Co, the terminal comes packed in two metal containers that double as shelters when the station is operating. The Transhorizon radio uses scattering of radio waves to provide reliable, bidirectional communication over 50 to 150 miles without intermediate relays for up to 12 voice or 96 teletypewriter messages. The terminal uses two 15-foot, dish-shaped antennas. Each antenna comes as an inflatable, balloonlike envelope, coated on one surface with aluminum to form a reflector. The complete assembly, including tower, weighs only 400 lbs and stores in a space of 3×2×7.5 feet.

—*Electrical Design News*, January 1958

LOOKING AROUND

AT ACQUISITION AS THE ULTIMATE WAY OF LICENSING IP

Just as we were beginning to enjoy a smoothly functioning market for silicon IP (intellectual property), a new trend is emerging. Large semiconductor companies and system developers are beginning to acquire—rather than simply license IP from—small IP vendors. As one large company puts it, the amount of information that must flow between design teams to successfully integrate one company's IP into another company's design is simply too large, given the social, practical, and legal barriers to information flow between corporations. As IP and design flows both become more complex, we may have to either rethink our concepts of trade secrets and patent protection or wave goodbye to a vibrant third-party-IP market.

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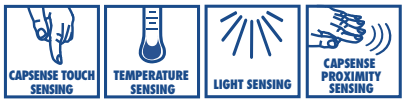

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